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MS-7B51

ATX
Ver: 1.0

CFL Platform

CPU:

Coffee lake S 95W

System Chipset:

Z390 PCH_H

Onboard Chip:

HD Audio Codec:ALC892-CG

LAN-Intel I219

SIO:NTC6797

Flash ROM: SPI 16 MB X1

VGA Output:

HDMI Port

DVI Port

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Main Memory:

*DDRIV (2666MHz) * 4 (Dual Channel)*

ACPI:

LDO

PWM:

IMVP8 -UPI9521

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 4*
*M.2 Slot * 2*
*CNVi Slot * 1*

Other:

*SATA3.0 *6*
*USB2.0 *6*
REAL USB3.1 Gen2 Type A+C
REAL USB3.1 Gen1 LAN_USB
*FRONT USB3.0 *4*

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MS-7B51

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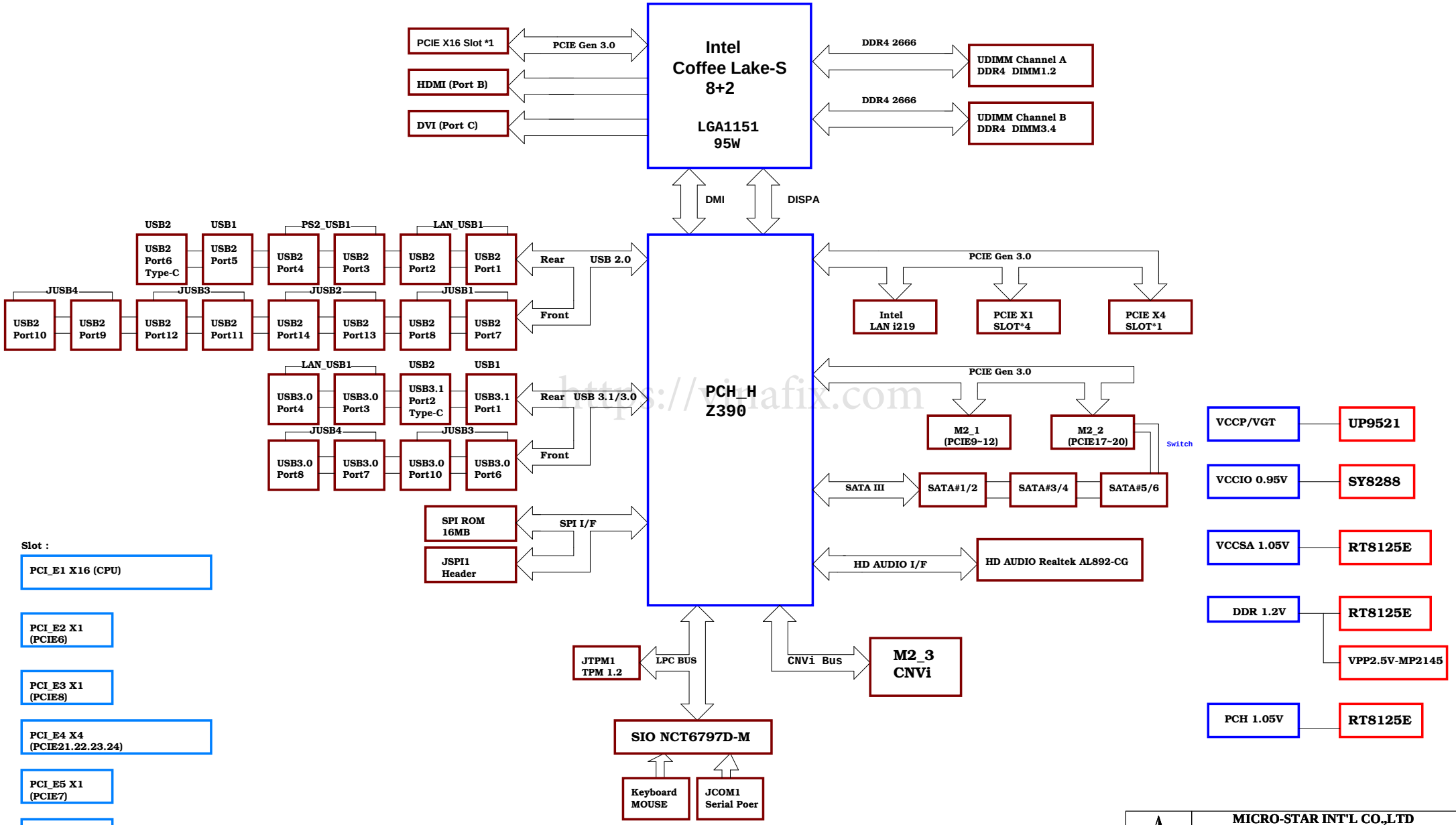
MS-7B51 Block Diagram



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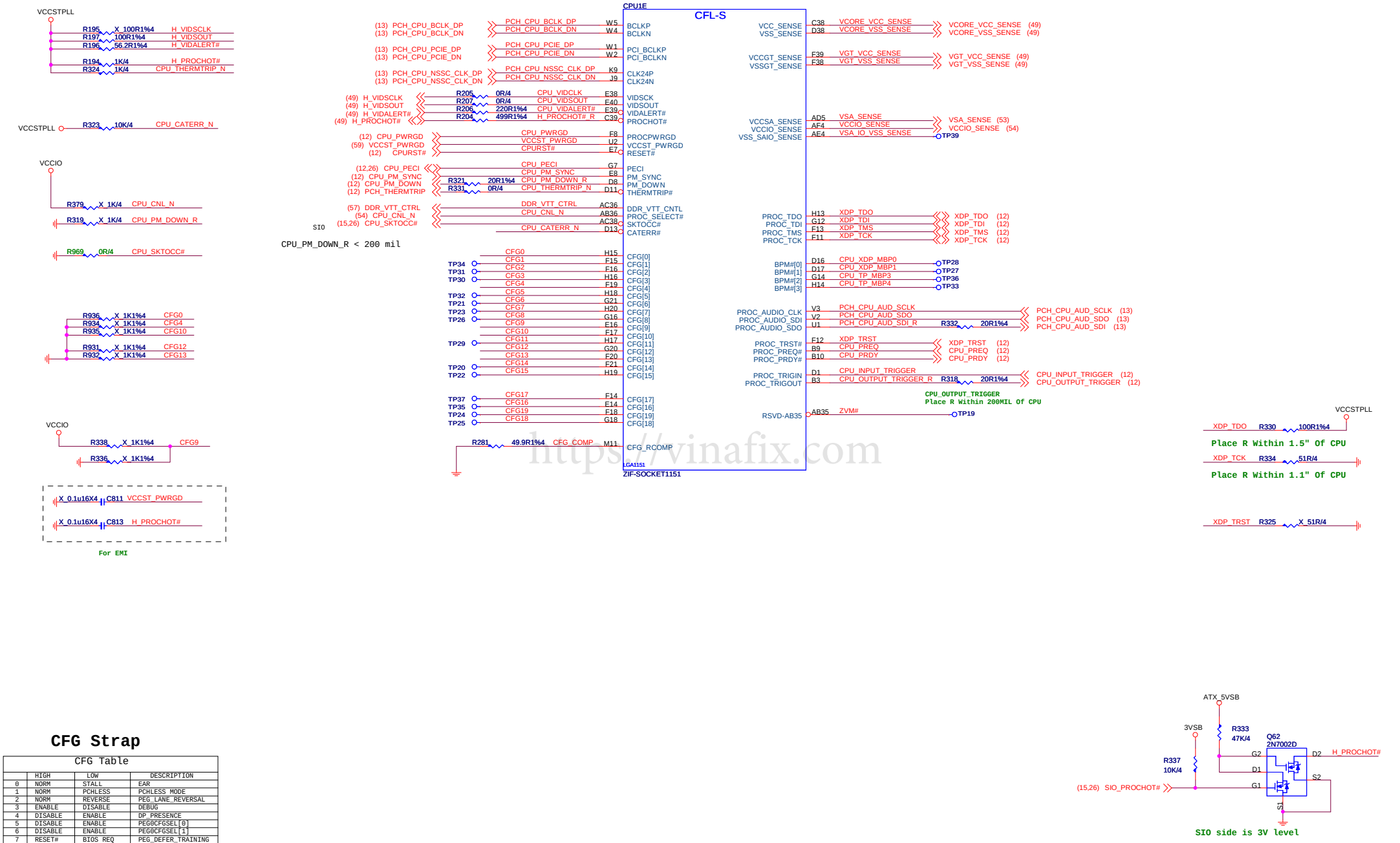

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CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	NORM	STALL	EAR
1	NORM	PCHLESS	PCHLESS MODE
2	NORM	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	DEBUG
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NO PRESENT	SVID NOT PRESENT
10	ACTIVATE	NO ACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC
12	SPT	NOT SPT	PCH TYPE
13	SVID	FIXED	VCCSA SVID
14	RSVD		
15	RSVD		

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MS-7B51	
Size: Custom	Document Description: CPU-Control/MISC/CFG
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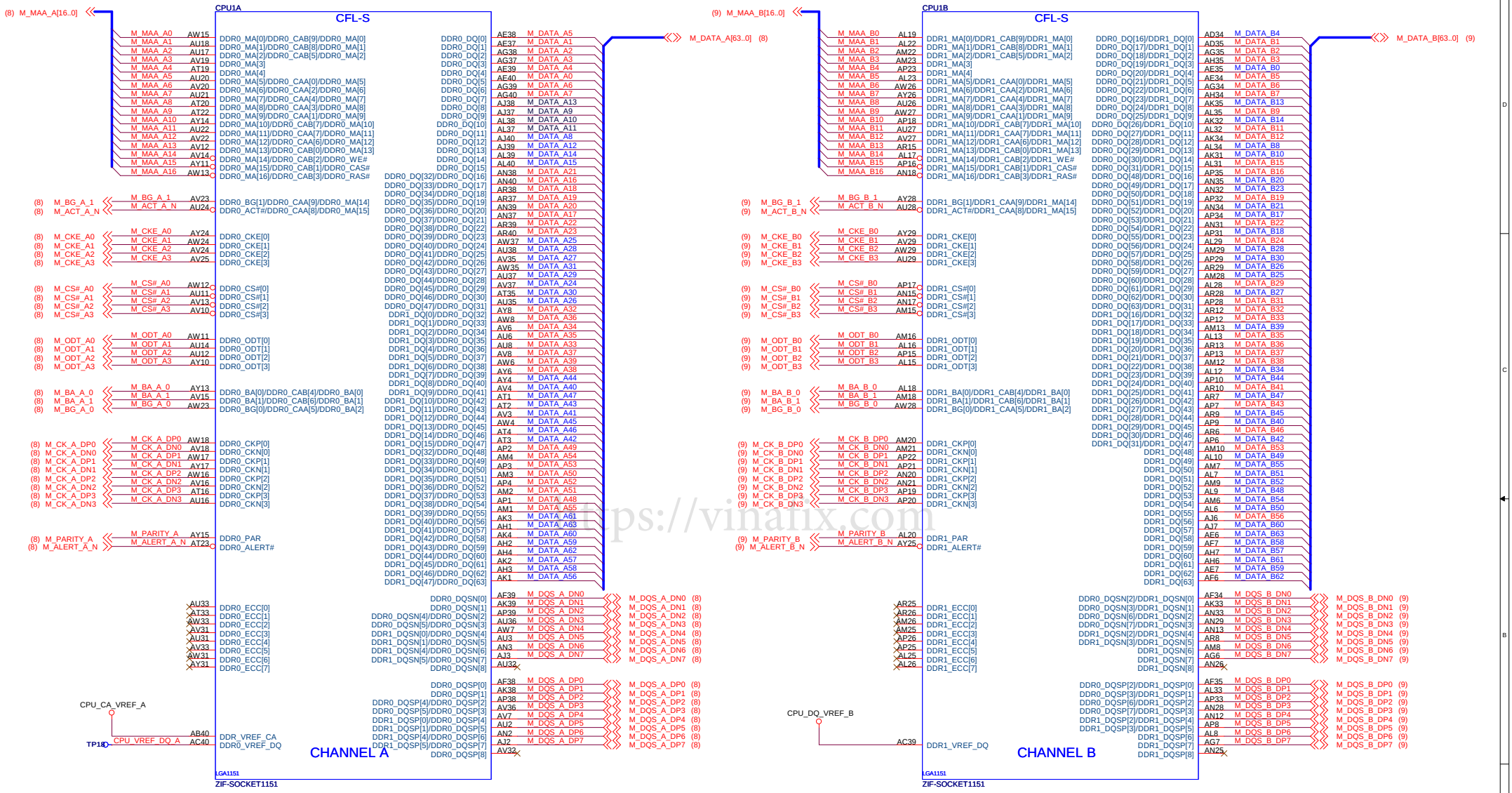
CPU1A
CFL-S
(8) M_MAA_A[16..0]
M_MAA_A0 AW15
M_MAA_A1 AU18
M_MAA_A2 AU17
M_MAA_A3 AV19
M_MAA_A4 AT19
M_MAA_A5 AU20
M_MAA_A6 AV20
M_MAA_A7 AU21
M_MAA_A8 AT20
M_MAA_A9 AT22
M_MAA_A10 AY14
M_MAA_A11 AU22
M_MAA_A12 AV22
M_MAA_A13 AV12
M_MAA_A14 AV14
M_MAA_A15 AY11
M_MAA_A16 AW13
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
DDR0_MA[14]/DDR0_CAB[2]/DDR0_WE#
DDR0_MA[15]/DDR0_CAB[1]/DDR0_CAS#
DDR0_MA[16]/DDR0_CAB[3]/DDR0_RAS#
(8) M_BG_A_1 AV23
(8) M_ACT_A_N AU24
DDR0_BG[1]/DDR0_CAA[9]/DDR0_MA[14]
DDR0_ACT#/DDR0_CAA[8]/DDR0_MA[15]
(8) M_CKE_A0 AY24
(8) M_CKE_A1 AW24
(8) M_CKE_A2 AY24
(8) M_CKE_A3 AV25
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
(8) M_CS#_A0 AW12
(8) M_CS#_A1 AU11
(8) M_CS#_A2 AV13
(8) M_CS#_A3 AV10
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
(8) M_ODT_A0 AW11
(8) M_ODT_A1 AU14
(8) M_ODT_A2 AU12
(8) M_ODT_A3 AY10
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
(8) M_BA_A_0 AY13
(8) M_BA_A_1 AV15
(8) M_BG_A_0 AW23
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_BG[0]/DDR0_CAA[5]/DDR0_BA[2]
(8) M_CK_A_DP0 AW18
(8) M_CK_A_DN0 AV18
(8) M_CK_A_DP1 AW17
(8) M_CK_A_DN1 AV17
(8) M_CK_A_DP2 AW16
(8) M_CK_A_DN2 AV16
(8) M_CK_A_DP3 AT16
(8) M_CK_A_DN3 AU16
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
(8) M_PARITY_A AY15
(8) M_ALERT_A_N AT23
DDR0_PAR
DDR0_ALERT#
AU33 DDR0_ECC[0]
AT33 DDR0_ECC[1]
AW33 DDR0_ECC[2]
AV31 DDR0_ECC[3]
AU31 DDR0_ECC[4]
AV33 DDR0_ECC[5]
AW31 DDR0_ECC[6]
AY31 DDR0_ECC[7]
CPU_CA_VREF_A
TP18
CPU_VREF_DQ_A AC40
AB40 DDR_VREF_CA
DDR0_VREF_DQ
DDR0_DQ[32]/DDR0_DQ[16]
DDR0_DQ[33]/DDR0_DQ[17]
DDR0_DQ[34]/DDR0_DQ[18]
DDR0_DQ[35]/DDR0_DQ[19]
DDR0_DQ[36]/DDR0_DQ[20]
DDR0_DQ[37]/DDR0_DQ[21]
DDR0_DQ[38]/DDR0_DQ[22]
DDR0_DQ[39]/DDR0_DQ[23]
DDR0_DQ[40]/DDR0_DQ[24]
DDR0_DQ[41]/DDR0_DQ[25]
DDR0_DQ[42]/DDR0_DQ[26]
DDR0_DQ[43]/DDR0_DQ[27]
DDR0_DQ[44]/DDR0_DQ[28]
DDR0_DQ[45]/DDR0_DQ[29]
DDR0_DQ[46]/DDR0_DQ[30]
DDR0_DQ[47]/DDR0_DQ[31]
DDR1_DQ[0]/DDR0_DQ[32]
DDR1_DQ[1]/DDR0_DQ[33]
DDR1_DQ[2]/DDR0_DQ[34]
DDR1_DQ[3]/DDR0_DQ[35]
DDR1_DQ[4]/DDR0_DQ[36]
DDR1_DQ[5]/DDR0_DQ[37]
DDR1_DQ[6]/DDR0_DQ[38]
DDR1_DQ[7]/DDR0_DQ[39]
DDR1_DQ[8]/DDR0_DQ[40]
DDR1_DQ[9]/DDR0_DQ[41]
DDR1_DQ[10]/DDR0_DQ[42]
DDR1_DQ[11]/DDR0_DQ[43]
DDR1_DQ[12]/DDR0_DQ[44]
DDR1_DQ[13]/DDR0_DQ[45]
DDR1_DQ[14]/DDR0_DQ[46]
DDR1_DQ[15]/DDR0_DQ[47]
DDR1_DQ[32]/DDR0_DQ[48]
DDR1_DQ[33]/DDR0_DQ[49]
DDR1_DQ[34]/DDR0_DQ[50]
DDR1_DQ[35]/DDR0_DQ[51]
DDR1_DQ[36]/DDR0_DQ[52]
DDR1_DQ[37]/DDR0_DQ[53]
DDR1_DQ[38]/DDR0_DQ[54]
DDR1_DQ[39]/DDR0_DQ[55]
DDR1_DQ[40]/DDR0_DQ[56]
DDR1_DQ[41]/DDR0_DQ[57]
DDR1_DQ[42]/DDR0_DQ[58]
DDR1_DQ[43]/DDR0_DQ[59]
DDR1_DQ[44]/DDR0_DQ[60]
DDR1_DQ[45]/DDR0_DQ[61]
DDR1_DQ[46]/DDR0_DQ[62]
DDR1_DQ[47]/DDR0_DQ[63]
DDR0_DQ[0] AE38 M_DATA_A5
DDR0_DQ[1] AE37 M_DATA_A1
DDR0_DQ[2] AG38 M_DATA_A2
DDR0_DQ[3] AG37 M_DATA_A3
DDR0_DQ[4] AE39 M_DATA_A4
DDR0_DQ[5] AE40 M_DATA_A0
DDR0_DQ[6] AG39 M_DATA_A6
DDR0_DQ[7] AG40 M_DATA_A7
DDR0_DQ[8] AJ38 M_DATA_A13
DDR0_DQ[9] AJ37 M_DATA_A9
DDR0_DQ[10] AL38 M_DATA_A10
DDR0_DQ[11] AL37 M_DATA_A11
DDR0_DQ[12] AJ40 M_DATA_A8
DDR0_DQ[13] AJ39 M_DATA_A12
DDR0_DQ[14] AL39 M_DATA_A14
DDR0_DQ[15] AL40 M_DATA_A15
DDR0_DQ[16] AN38 M_DATA_A21
DDR0_DQ[17] AN40 M_DATA_A16
DDR0_DQ[18] AR38 M_DATA_A18
DDR0_DQ[19] AR37 M_DATA_A19
DDR0_DQ[20] AN39 M_DATA_A20
DDR0_DQ[21] AN37 M_DATA_A17
DDR0_DQ[22] AP39 M_DATA_A22
DDR0_DQ[23] AR40 M_DATA_A23
DDR0_DQ[24] AW37 M_DATA_A25
DDR0_DQ[25] AU38 M_DATA_A28
DDR0_DQ[26] AV35 M_DATA_A27
DDR0_DQ[27] AW35 M_DATA_A31
DDR0_DQ[28] AU37 M_DATA_A29
DDR0_DQ[29] AV37 M_DATA_A24
DDR0_DQ[30] AT35 M_DATA_A30
DDR0_DQ[31] AU35 M_DATA_A26
DDR0_DQ[32] AY8 M_DATA_A32
DDR0_DQ[33] AW8 M_DATA_A36
DDR0_DQ[34] AV6 M_DATA_A34
DDR0_DQ[35] AU6 M_DATA_A35
DDR0_DQ[36] AU8 M_DATA_A33
DDR0_DQ[37] AV8 M_DATA_A37
DDR0_DQ[38] AW6 M_DATA_A39
DDR0_DQ[39] AY6 M_DATA_A38
DDR0_DQ[40] AY4 M_DATA_A44
DDR0_DQ[41] AV4 M_DATA_A40
DDR0_DQ[42] AT1 M_DATA_A47
DDR0_DQ[43] AT2 M_DATA_A43
DDR0_DQ[44] AV3 M_DATA_A41
DDR0_DQ[45] AW4 M_DATA_A45
DDR0_DQ[46] AT4 M_DATA_A46
DDR0_DQ[47] AT3 M_DATA_A42
DDR0_DQ[48] AP2 M_DATA_A49
DDR0_DQ[49] AM4 M_DATA_A54
DDR0_DQ[50] AP3 M_DATA_A53
DDR0_DQ[51] AM3 M_DATA_A50
DDR0_DQ[52] AP4 M_DATA_A52
DDR0_DQ[53] AM2 M_DATA_A51
DDR0_DQ[54] AP1 M_DATA_A48
DDR0_DQ[55] AM1 M_DATA_A55
DDR0_DQ[56] AK3 M_DATA_A61
DDR0_DQ[57] AH1 M_DATA_A63
DDR0_DQ[58] AK4 M_DATA_A60
DDR0_DQ[59] AH2 M_DATA_A59
DDR0_DQ[60] AH4 M_DATA_A62
DDR0_DQ[61] AK2 M_DATA_A57
DDR0_DQ[62] AH3 M_DATA_A58
DDR0_DQ[63] AK1 M_DATA_A56
M_DATA_A[63..0] (8)
DDR0_DQSN[0] AF39 M_DQS_A_DN0
DDR0_DQSN[1] AK39 M_DQS_A_DN1
DDR0_DQSN[2] AP39 M_DQS_A_DN2
DDR0_DQSN[3] AU36 M_DQS_A_DN3
DDR0_DQSN[4] AW7 M_DQS_A_DN4
DDR0_DQSN[5] AU3 M_DQS_A_DN5
DDR0_DQSN[6] AN3 M_DQS_A_DN6
DDR0_DQSN[7] AJ3 M_DQS_A_DN7
DDR0_DQSN[8] AU32
DDR0_DQSP[0] AF38 M_DQS_A_DP0
DDR0_DQSP[1] AK38 M_DQS_A_DP1
DDR0_DQSP[2] AP38 M_DQS_A_DP2
DDR0_DQSP[3] AV36 M_DQS_A_DP3
DDR0_DQSP[4] AV7 M_DQS_A_DP4
DDR0_DQSP[5] AU2 M_DQS_A_DP5
DDR0_DQSP[6] AN2 M_DQS_A_DP6
DDR0_DQSP[7] AJ2 M_DQS_A_DP7
DDR0_DQSP[8] AV32
M_DQS_A_DN0 (8)
M_DQS_A_DN1 (8)
M_DQS_A_DN2 (8)
M_DQS_A_DN3 (8)
M_DQS_A_DN4 (8)
M_DQS_A_DN5 (8)
M_DQS_A_DN6 (8)
M_DQS_A_DN7 (8)
M_DQS_A_DP0 (8)
M_DQS_A_DP1 (8)
M_DQS_A_DP2 (8)
M_DQS_A_DP3 (8)
M_DQS_A_DP4 (8)
M_DQS_A_DP5 (8)
M_DQS_A_DP6 (8)
M_DQS_A_DP7 (8)
CHANNEL A
LGA1151
ZIF-SOCKET1151
CPU1B
CFL-S
(9) M_MAA_B[16..0]
M_MAA_B0 AL19
M_MAA_B1 AL22
M_MAA_B2 AM22
M_MAA_B3 AM23
M_MAA_B4 AP23
M_MAA_B5 AL23
M_MAA_B6 AW26
M_MAA_B7 AY26
M_MAA_B8 AU26
M_MAA_B9 AW27
M_MAA_B10 AP18
M_MAA_B11 AU27
M_MAA_B12 AV27
M_MAA_B13 AR15
M_MAA_B14 AL17
M_MAA_B15 AP16
M_MAA_B16 AN18
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAB[2]/DDR1_WE#
DDR1_MA[15]/DDR1_CAB[1]/DDR1_CAS#
DDR1_MA[16]/DDR1_CAB[3]/DDR1_RAS#
(9) M_BG_B_1 AY28
(9) M_ACT_B_N AU28
DDR1_BG[1]/DDR1_CAA[9]/DDR1_MA[14]
DDR1_ACT#/DDR1_CAA[8]/DDR1_MA[15]
(9) M_CKE_B0 AY29
(9) M_CKE_B1 AV29
(9) M_CKE_B2 AW29
(9) M_CKE_B3 AU29
DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]
(9) M_CS#_B0 AP17
(9) M_CS#_B1 AN15
(9) M_CS#_B2 AN17
(9) M_CS#_B3 AM15
DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
(9) M_ODT_B0 AM16
(9) M_ODT_B1 AL16
(9) M_ODT_B2 AP15
(9) M_ODT_B3 AL15
DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
(9) M_BA_B_0 AL18
(9) M_BA_B_1 AM18
(9) M_BG_B_0 AW28
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BG[0]/DDR1_CAA[5]/DDR1_BA[2]
(9) M_CK_B_DP0 AM20
(9) M_CK_B_DN0 AM21
(9) M_CK_B_DP1 AP22
(9) M_CK_B_DN1 AP21
(9) M_CK_B_DP2 AN20
(9) M_CK_B_DN2 AN21
(9) M_CK_B_DP3 AP19
(9) M_CK_B_DN3 AP20
DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
(9) M_PARITY_B AL20
(9) M_ALERT_B_N AY25
DDR1_PAR
DDR1_ALERT#
AR25 DDR1_ECC[0]
AR26 DDR1_ECC[1]
AM26 DDR1_ECC[2]
AM25 DDR1_ECC[3]
AP26 DDR1_ECC[4]
AP25 DDR1_ECC[5]
AL25 DDR1_ECC[6]
AL26 DDR1_ECC[7]
CPU_DQ_VREF_B
AC39 DDR1_VREF_DQ
DDR0_DQ[16]/DDR1_DQ[0] AD34 M_DATA_B4
DDR0_DQ[17]/DDR1_DQ[1] AD35 M_DATA_B1
DDR0_DQ[18]/DDR1_DQ[2] AG35 M_DATA_B2
DDR0_DQ[19]/DDR1_DQ[3] AH35 M_DATA_B3
DDR0_DQ[20]/DDR1_DQ[4] AE35 M_DATA_B0
DDR0_DQ[21]/DDR1_DQ[5] AE34 M_DATA_B5
DDR0_DQ[22]/DDR1_DQ[6] AG34 M_DATA_B6
DDR0_DQ[23]/DDR1_DQ[7] AH34 M_DATA_B7
DDR0_DQ[24]/DDR1_DQ[8] AK35 M_DATA_B13
DDR0_DQ[25]/DDR1_DQ[9] AL35 M_DATA_B9
DDR0_DQ[26]/DDR1_DQ[10] AK32 M_DATA_B14
DDR0_DQ[27]/DDR1_DQ[11] AL32 M_DATA_B11
DDR0_DQ[28]/DDR1_DQ[12] AK34 M_DATA_B12
DDR0_DQ[29]/DDR1_DQ[13] AL34 M_DATA_B8
DDR0_DQ[30]/DDR1_DQ[14] AK31 M_DATA_B10
DDR0_DQ[31]/DDR1_DQ[15] AL31 M_DATA_B15
DDR0_DQ[48]/DDR1_DQ[16] AP35 M_DATA_B16
DDR0_DQ[49]/DDR1_DQ[17] AN35 M_DATA_B20
DDR0_DQ[50]/DDR1_DQ[18] AN32 M_DATA_B23
DDR0_DQ[51]/DDR1_DQ[19] AP32 M_DATA_B19
DDR0_DQ[52]/DDR1_DQ[20] AN34 M_DATA_B21
DDR0_DQ[53]/DDR1_DQ[21] AP34 M_DATA_B17
DDR0_DQ[54]/DDR1_DQ[22] AN31 M_DATA_B22
DDR0_DQ[55]/DDR1_DQ[23] AP31 M_DATA_B18
DDR0_DQ[56]/DDR1_DQ[24] AL29 M_DATA_B24
DDR0_DQ[57]/DDR1_DQ[25] AM29 M_DATA_B28
DDR0_DQ[58]/DDR1_DQ[26] AP29 M_DATA_B30
DDR0_DQ[59]/DDR1_DQ[27] AR29 M_DATA_B26
DDR0_DQ[60]/DDR1_DQ[28] AM28 M_DATA_B25
DDR0_DQ[61]/DDR1_DQ[29] AL28 M_DATA_B29
DDR0_DQ[62]/DDR1_DQ[30] AP28 M_DATA_B27
DDR0_DQ[63]/DDR1_DQ[31] AP28 M_DATA_B31
DDR1_DQ[16]/DDR1_DQ[32] AR12 M_DATA_B32
DDR1_DQ[17]/DDR1_DQ[33] AP12 M_DATA_B33
DDR1_DQ[18]/DDR1_DQ[34] AM13 M_DATA_B39
DDR1_DQ[19]/DDR1_DQ[35] AL13 M_DATA_B35
DDR1_DQ[20]/DDR1_DQ[36] AR13 M_DATA_B36
DDR1_DQ[21]/DDR1_DQ[37] AP13 M_DATA_B37
DDR1_DQ[22]/DDR1_DQ[38] AM12 M_DATA_B38
DDR1_DQ[23]/DDR1_DQ[39] AL12 M_DATA_B34
DDR1_DQ[24]/DDR1_DQ[40] AP10 M_DATA_B44
DDR1_DQ[25]/DDR1_DQ[41] AR10 M_DATA_B41
DDR1_DQ[26]/DDR1_DQ[42] AR7 M_DATA_B47
DDR1_DQ[27]/DDR1_DQ[43] AP7 M_DATA_B43
DDR1_DQ[28]/DDR1_DQ[44] AR9 M_DATA_B45
DDR1_DQ[29]/DDR1_DQ[45] AP9 M_DATA_B40
DDR1_DQ[30]/DDR1_DQ[46] AR6 M_DATA_B46
DDR1_DQ[31]/DDR1_DQ[47] AP6 M_DATA_B42
DDR1_DQ[48] AM10 M_DATA_B53
DDR1_DQ[49] AL10 M_DATA_B49
DDR1_DQ[50] AM7 M_DATA_B55
DDR1_DQ[51] AL7 M_DATA_B51
DDR1_DQ[52] AM9 M_DATA_B52
DDR1_DQ[53] AL9 M_DATA_B48
DDR1_DQ[54] AM6 M_DATA_B54
DDR1_DQ[55] AL6 M_DATA_B50
DDR1_DQ[56] AJ6 M_DATA_B56
DDR1_DQ[57] AJ7 M_DATA_B60
DDR1_DQ[58] AE6 M_DATA_B63
DDR1_DQ[59] AF7 M_DATA_B58
DDR1_DQ[60] AH7 M_DATA_B57
DDR1_DQ[61] AH6 M_DATA_B61
DDR1_DQ[62] AE7 M_DATA_B59
DDR1_DQ[63] AF6 M_DATA_B62
M_DATA_B[63..0] (9)
DDR0_DQSN[2]/DDR1_DQSN[0] AF34 M_DQS_B_DN0
DDR0_DQSN[3]/DDR1_DQSN[1] AK33 M_DQS_B_DN1
DDR0_DQSN[6]/DDR1_DQSN[2] AN33 M_DQS_B_DN2
DDR0_DQSN[7]/DDR1_DQSN[3] AN29 M_DQS_B_DN3
DDR1_DQSN[2]/DDR1_DQSN[4] AN13 M_DQS_B_DN4
DDR1_DQSN[3]/DDR1_DQSN[5] AR8 M_DQS_B_DN5
DDR1_DQSN[6] AM8 M_DQS_B_DN6
DDR1_DQSN[7] AG6 M_DQS_B_DN7
DDR1_DQSN[8] AN26
DDR0_DQSP[2]/DDR1_DQSP[0] AE35 M_DQS_B_DP0
DDR0_DQSP[3]/DDR1_DQSP[1] AL33 M_DQS_B_DP1
DDR0_DQSP[6]/DDR1_DQSP[2] AP33 M_DQS_B_DP2
DDR0_DQSP[7]/DDR1_DQSP[3] AN28 M_DQS_B_DP3
DDR1_DQSP[2]/DDR1_DQSP[4] AN12 M_DQS_B_DP4
DDR1_DQSP[3]/DDR1_DQSP[5] AP8 M_DQS_B_DP5
DDR1_DQSP[6] AL8 M_DQS_B_DP6
DDR1_DQSP[7] AG7 M_DQS_B_DP7
DDR1_DQSP[8] AN25
M_DQS_B_DN0 (9)
M_DQS_B_DN1 (9)
M_DQS_B_DN2 (9)
M_DQS_B_DN3 (9)
M_DQS_B_DN4 (9)
M_DQS_B_DN5 (9)
M_DQS_B_DN6 (9)
M_DQS_B_DN7 (9)
M_DQS_B_DP0 (9)
M_DQS_B_DP1 (9)
M_DQS_B_DP2 (9)
M_DQS_B_DP3 (9)
M_DQS_B_DP4 (9)
M_DQS_B_DP5 (9)
M_DQS_B_DP6 (9)
M_DQS_B_DP7 (9)
CHANNEL B
LGA1151
ZIF-SOCKET1151
Socket PN N12-151A010-L06
https://vinafix.com
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MICRO-STAR INT'L CO.,LTD
MS-7B51
Size Custom
Document Description CPU-Memory
Rev 1.0
Date: Tuesday, May 22, 2018
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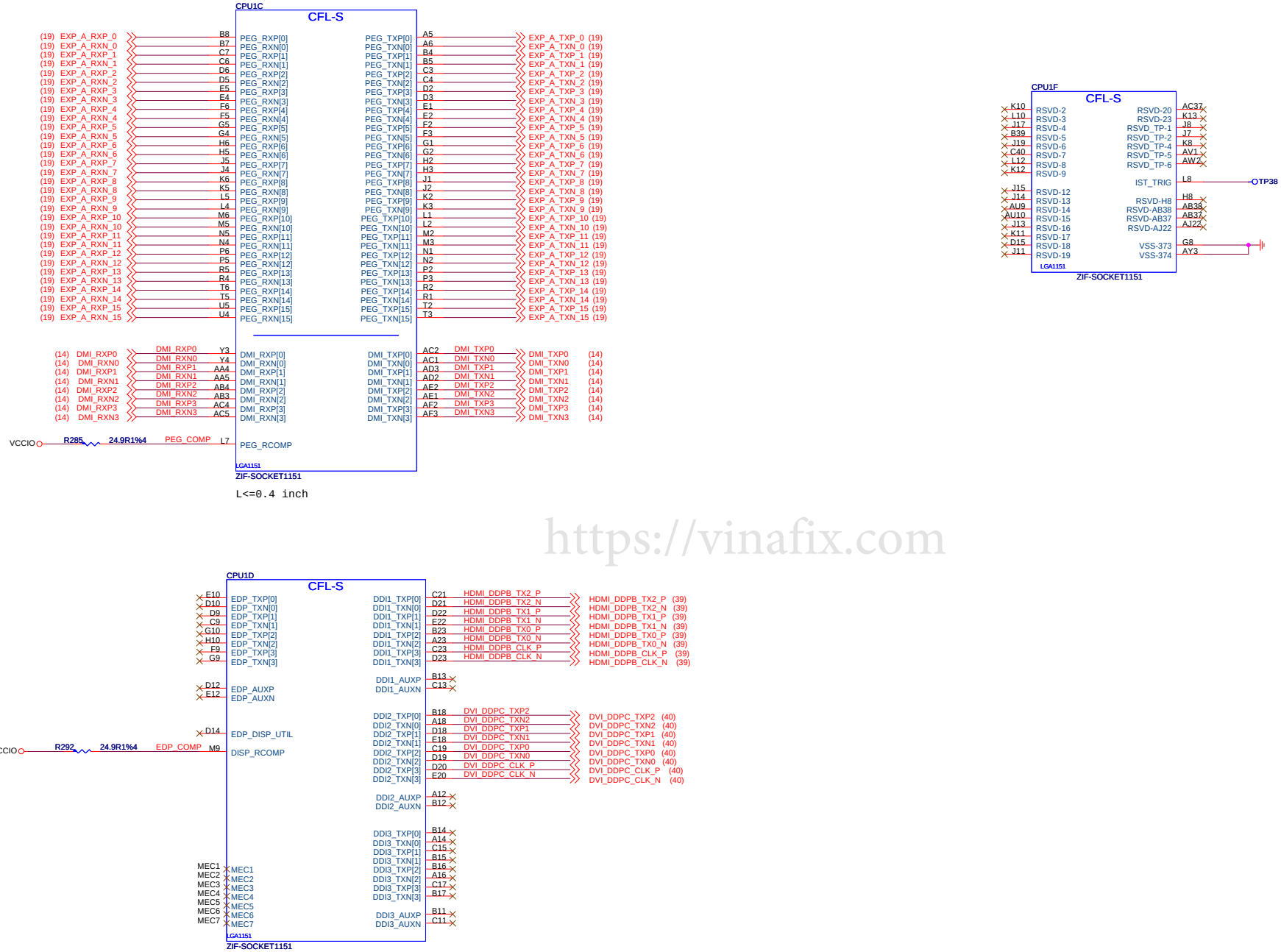

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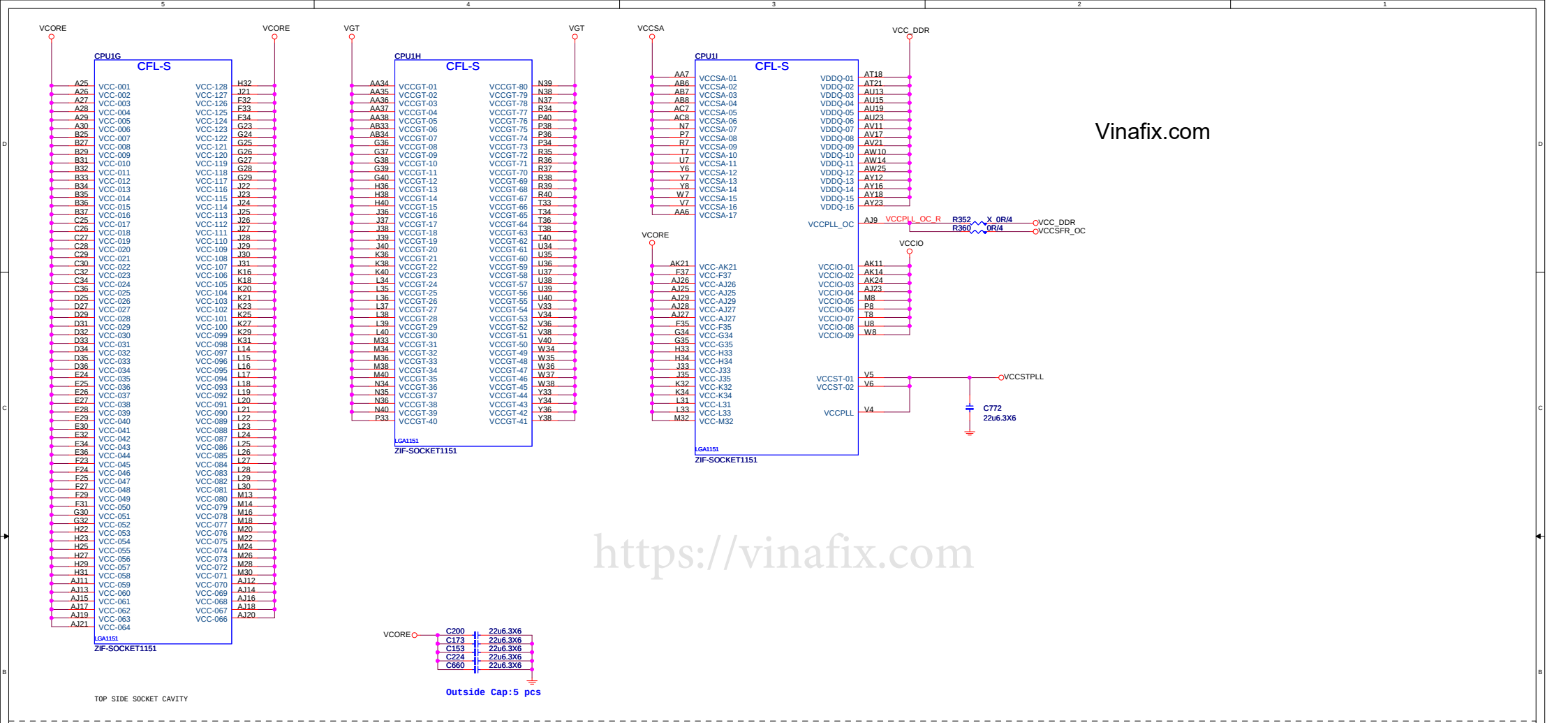
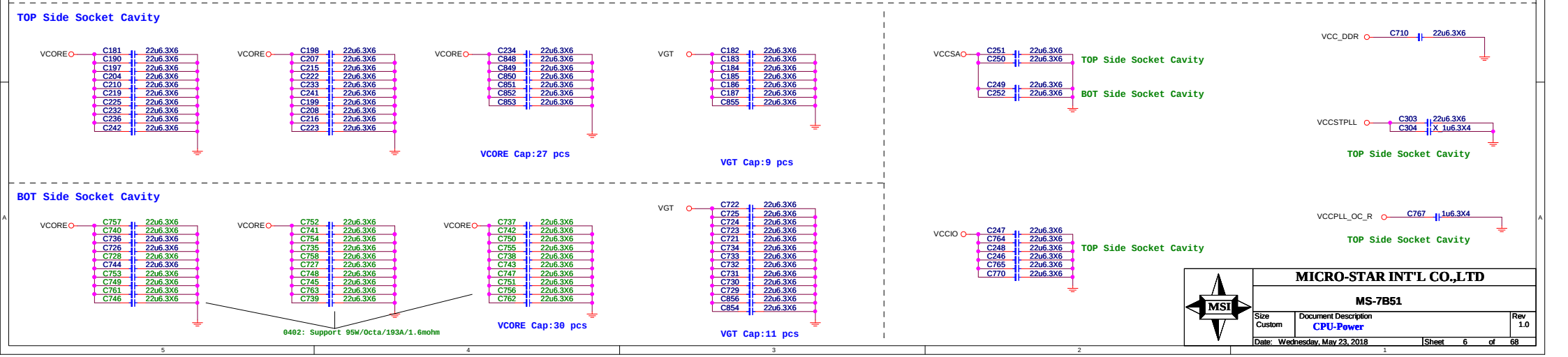
MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: CPU-PEG/Display/RSD
Rev: 1.0	
Date: Tuesday, May 22, 2018	Sheet 5 of 68





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Size	Document Description	Rev
Custom	CPU-Power	1.0

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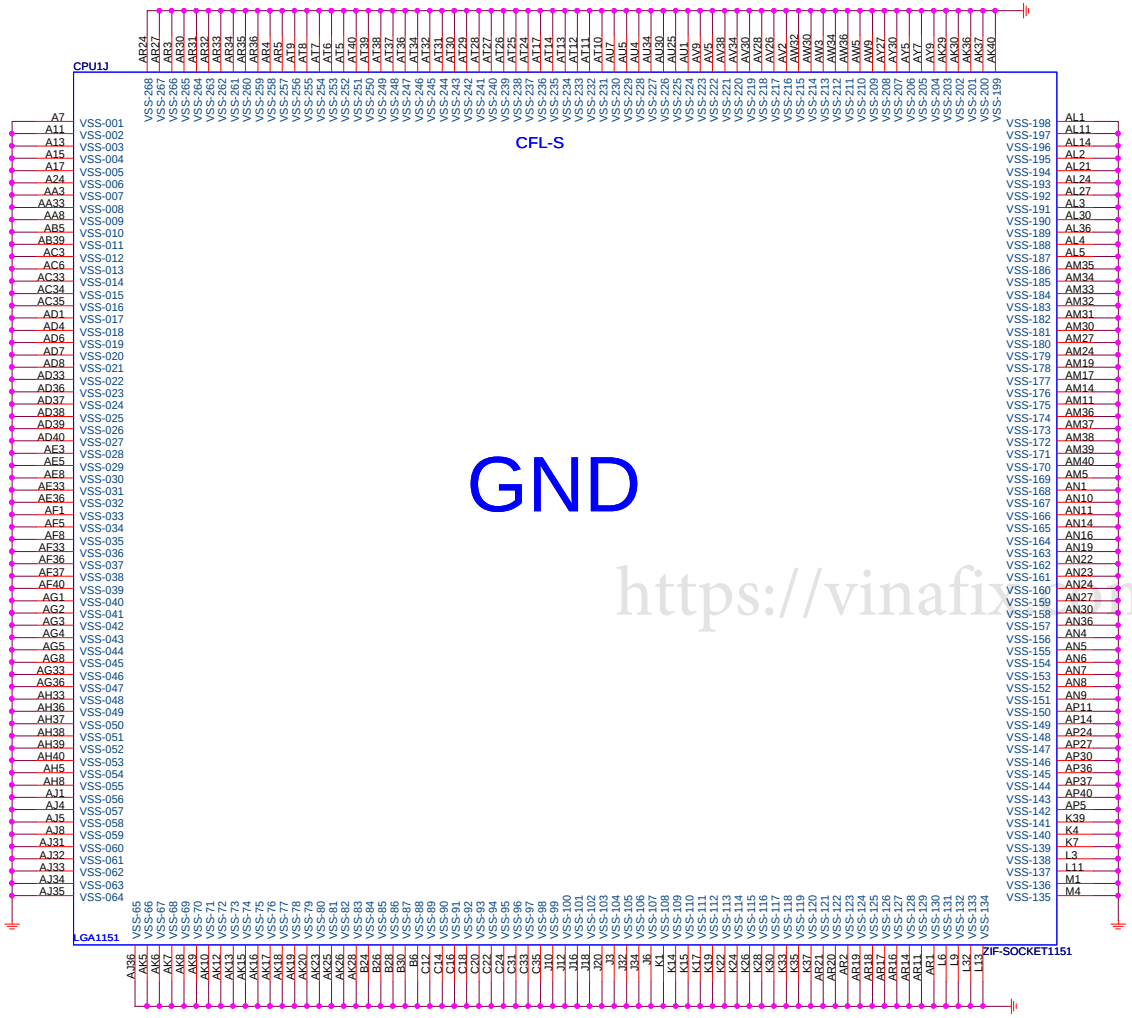

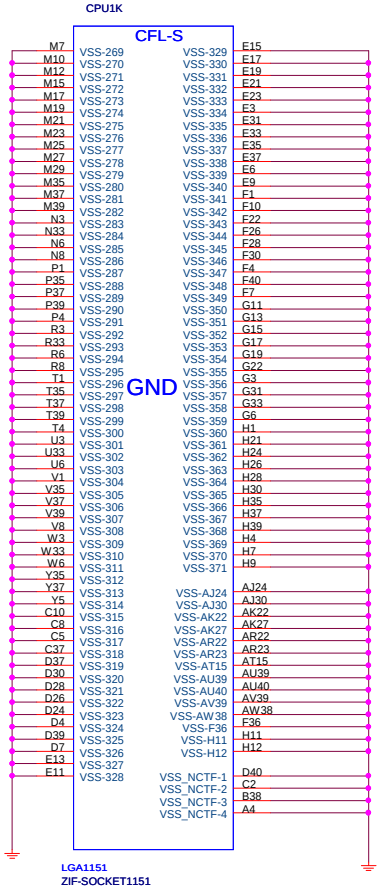

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MICRO-STAR INT'L CO.,LTD		
MS-7B51		
Size: Custom	Document Description: CPU-GND	Rev: 1.0
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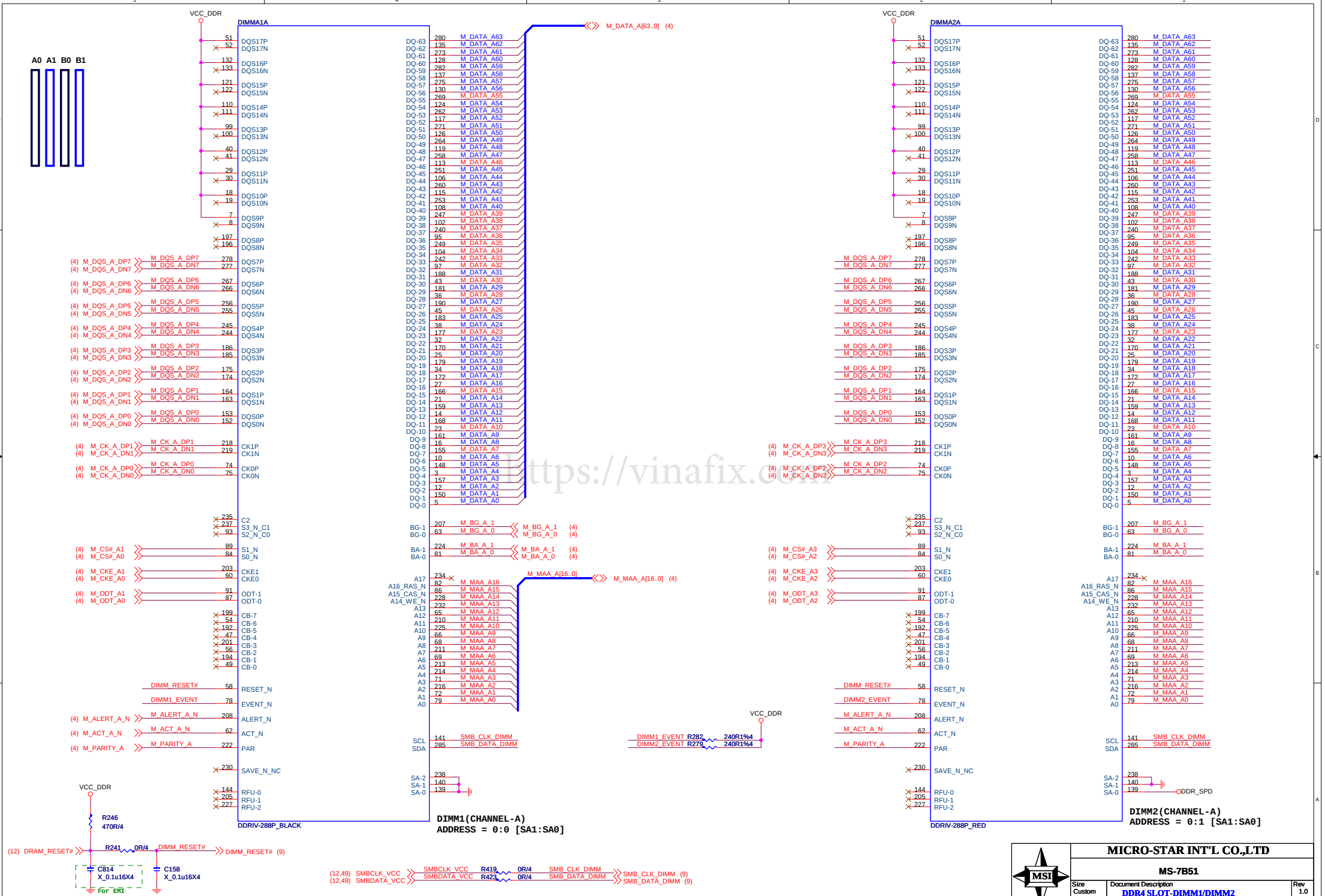

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MICRO-STAR INT'L CO.,LTD

MS-7B51

Size	Document Description	Rev
Custom	DDR4 SLOT-DIMM1/DIMM2	1.0

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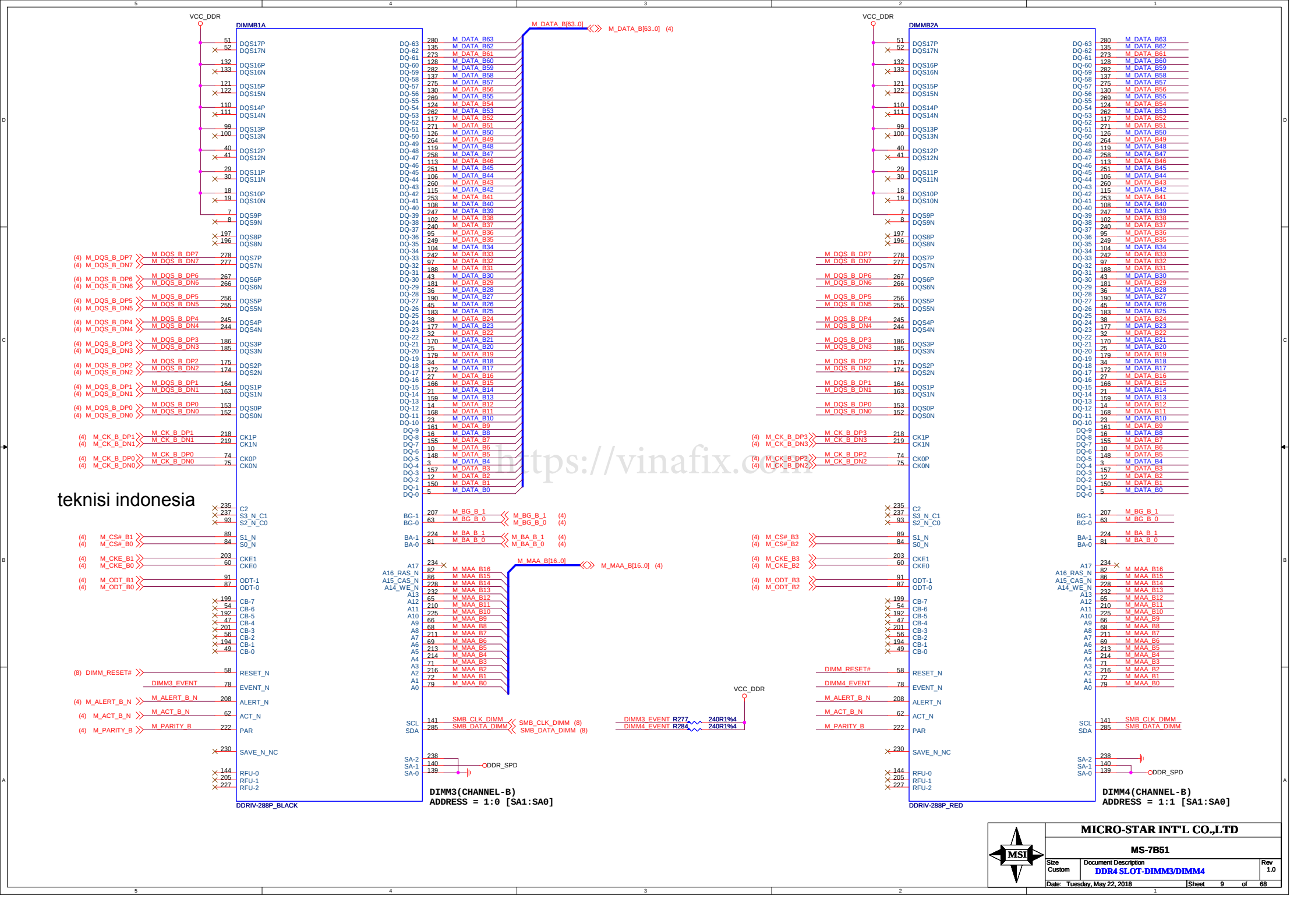

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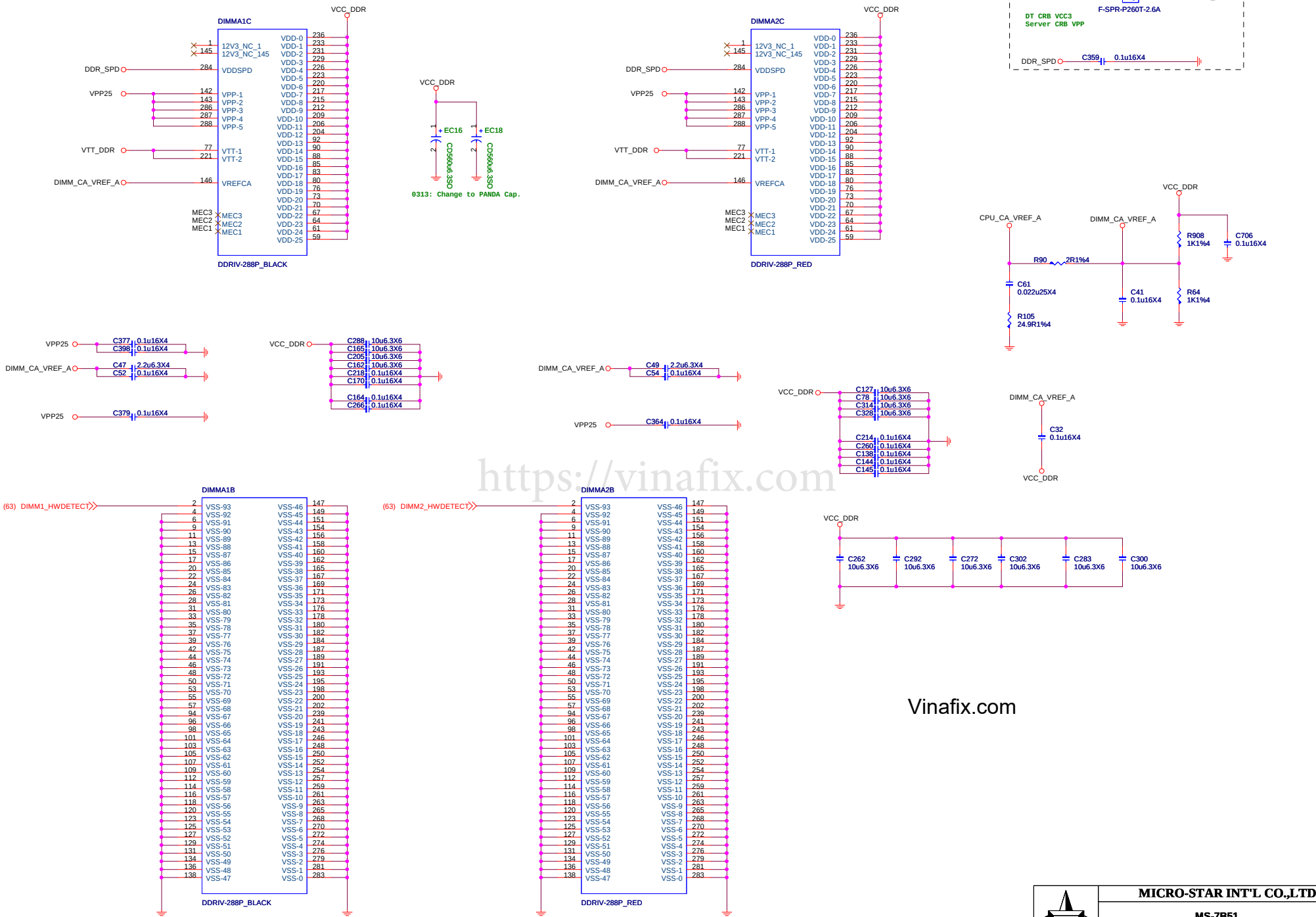
MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: DDR4 SLOT-DIMM3/DIMM4
Rev: 1.0	
Date: Tuesday, May 22, 2018	Sheet 9 of 68



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MS-7B51

Size	Document Description	Rev
Custom	DDR4-POWER/GND-1	1.0

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MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: DDR4-POWER/GND-2
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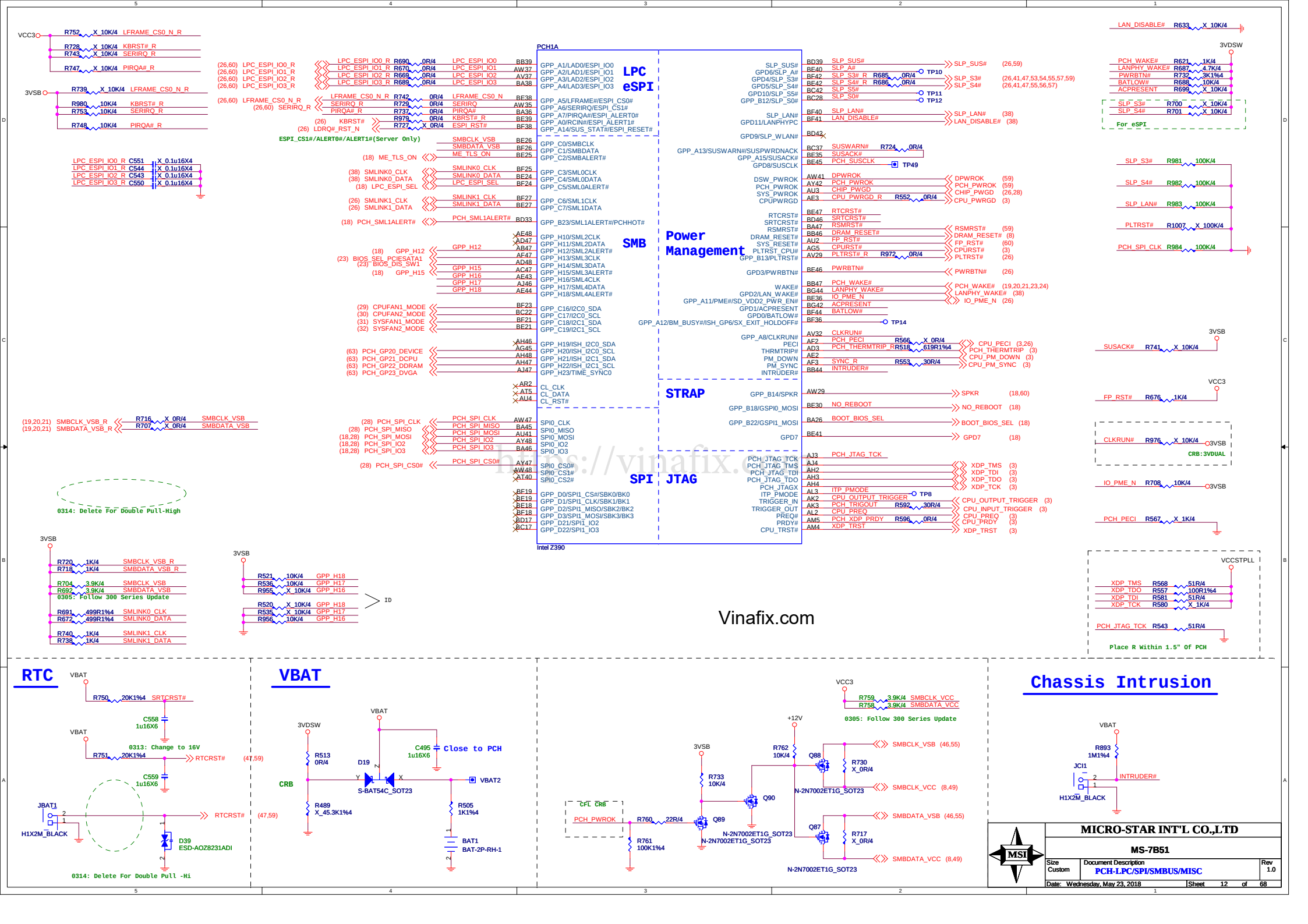
Date: Tuesday, May 22, 2018	Sheet 11 of 68


PCH1A
LPC eSPI
SMB
Power Management
STRAP
SPI
JTAG
Intel Z390
RTC
VBAT
Chassis Intrusion
0314: Delete For Double Pull-High
0305: Follow 300 Series Update
0313: Change to 16V
0314: Delete For Double Pull -Hi
Close to PCH
S-BAT54C_SOT23
ESD-AOZ8231ADI
BAT-2P-RH-1
H1X2M_BLACK
N-2N7002ET1G_SOT23
Place R Within 1.5" Of PCH
MICRO-STAR INT'L CO.,LTD
MS-7B51
PCH-LPC/SPI/SMBUS/MISC
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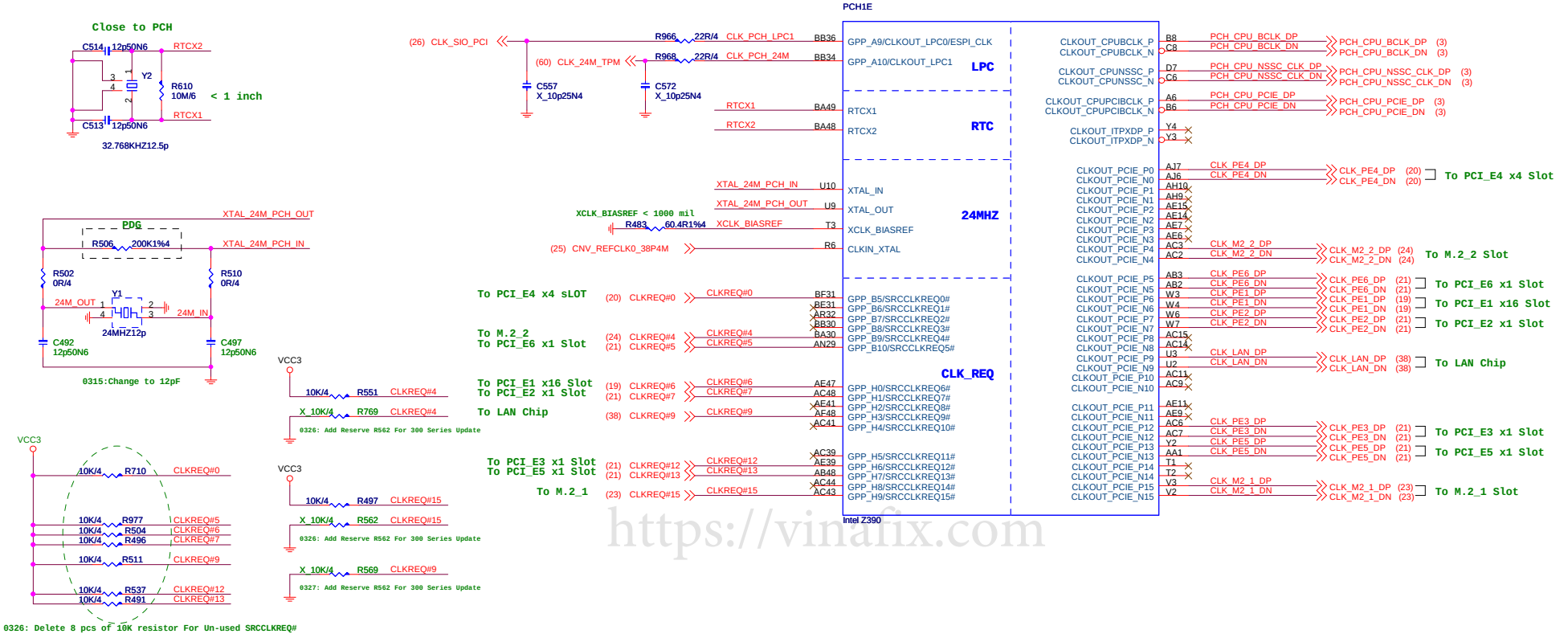
PCH_CLK



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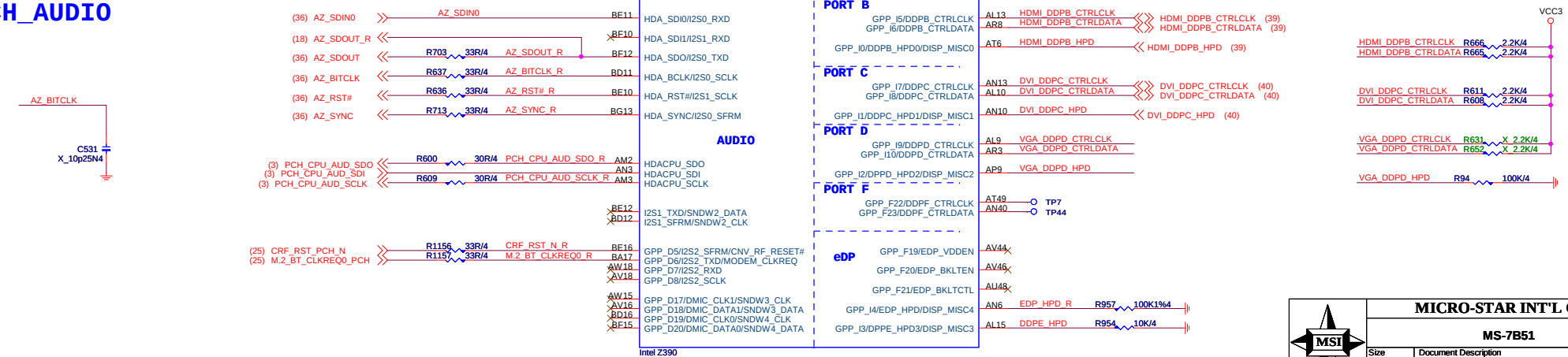
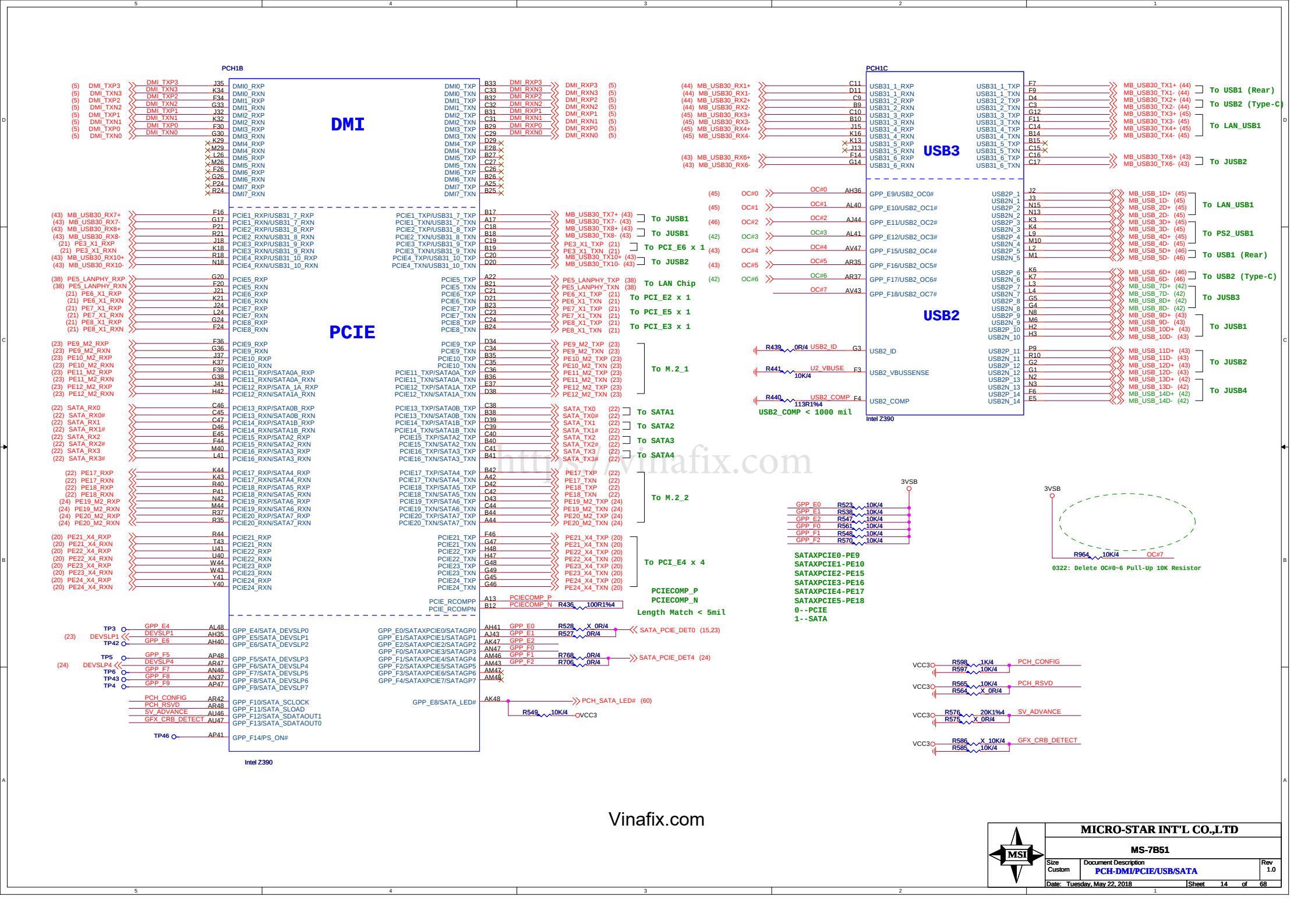
PCH_AUDIO



MICRO-STAR INT'L CO.,LTD		
MS-7B51		
Size: Custom	Document Description: PCH-Clock/Audio	Rev: 1.0
Date: Wednesday, May 23, 2018	Sheet 13 of 68	



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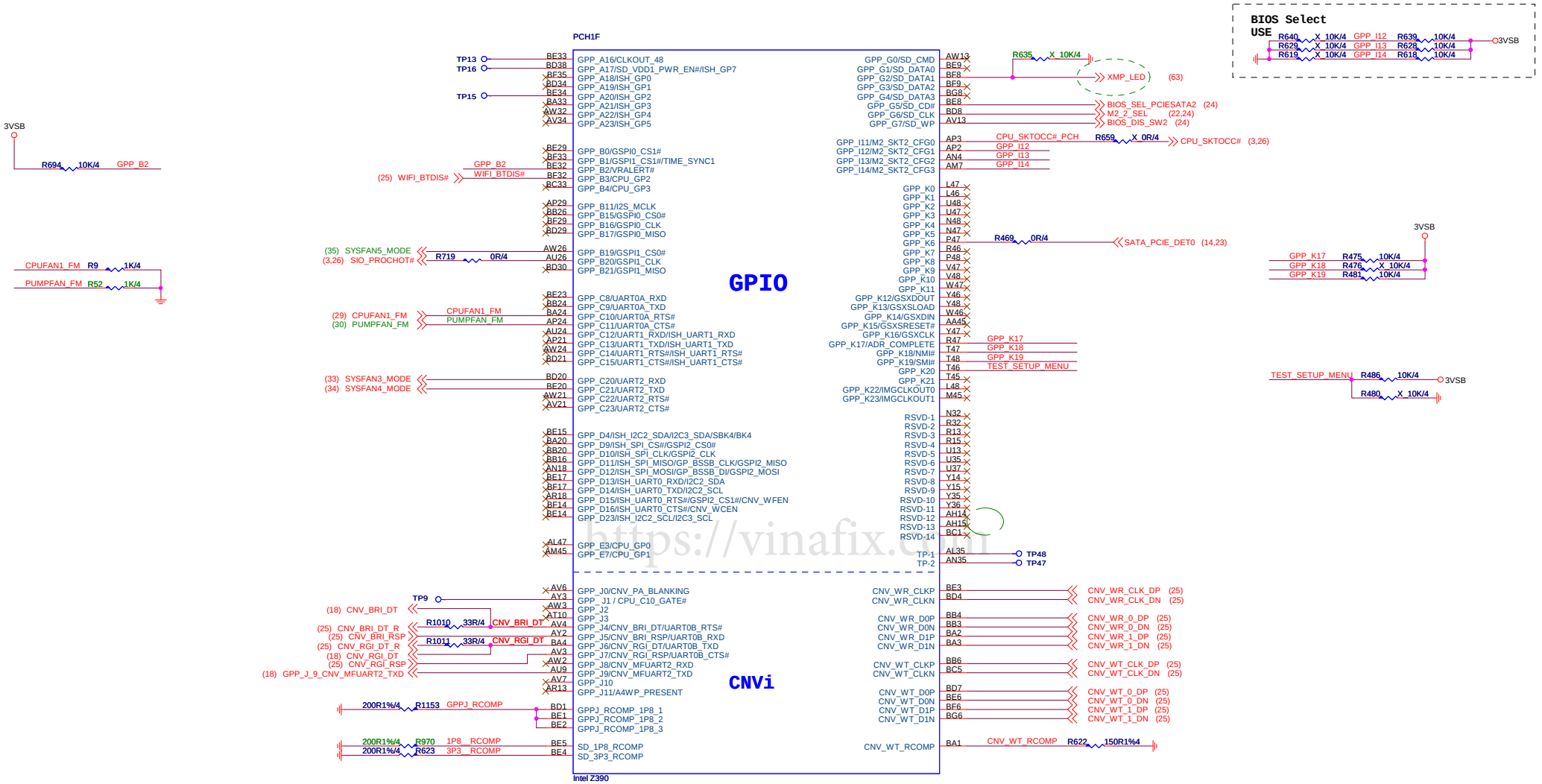
MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: PCH-DMI/PCIE/USB/SATA
Rev: 1.0	
Date: Tuesday, May 22, 2018	Sheet 14 of 68


PCH1F
GPIO
CNVi
Intel Z390
BIOS Select
USE
3VSB
GPP_A16/CLKOUT_48
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_B0/GSPI0_CS1#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B2/VRALERT#
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_B11/I2S_MCLK
GPP_B15/GSPI0_CS0#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B19/GSPI1_CS0#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_C8/UART0A_RXD
GPP_C9/UART0A_TXD
GPP_C10/UART0A_RTS#
GPP_C11/UART0A_CTS#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_D23/ISH_I2C2_SCL/I2C3_SCL
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_J0/CNV_PA_BLANKING
GPP_ J1 / CPU_C10_GATE#
GPP_J2
GPP_J3
GPP_J4/CNV_BRI_DT/UART0B_RTS#
GPP_J5/CNV_BRI_RSP/UART0B_RXD
GPP_J6/CNV_RGI_DT/UART0B_TXD
GPP_J7/CNV_RGI_RSP/UART0B_CTS#
GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD
GPP_J10
GPP_J11/A4WP_PRESENT
GPPJ_RCOMP_1P8_1
GPPJ_RCOMP_1P8_2
GPPJ_RCOMP_1P8_3
SD_1P8_RCOMP
SD_3P3_RCOMP
GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_I11/M2_SKT2_CFG0
GPP_I12/M2_SKT2_CFG1
GPP_I13/M2_SKT2_CFG2
GPP_I14/M2_SKT2_CFG3
GPP_K0
GPP_K1
GPP_K2
GPP_K3
GPP_K4
GPP_K5
GPP_K6
GPP_K7
GPP_K8
GPP_K9
GPP_K10
GPP_K11
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
GPP_K16/GSXCLK
GPP_K17/ADR_COMPLETE
GPP_K18/NMI#
GPP_K19/SMI#
GPP_K20
GPP_K21
GPP_K22/IMGCLKOUT0
GPP_K23/IMGCLKOUT1
RSVD-1
RSVD-2
RSVD-3
RSVD-4
RSVD-5
RSVD-6
RSVD-7
RSVD-8
RSVD-9
RSVD-10
RSVD-11
RSVD-12
RSVD-13
RSVD-14
TP-1
TP-2
CNV_WR_CLKP
CNV_WR_CLKN
CNV_WR_D0P
CNV_WR_D0N
CNV_WR_D1P
CNV_WR_D1N
CNV_WT_CLKP
CNV_WT_CLKN
CNV_WT_D0P
CNV_WT_D0N
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_RCOMP
XMP_LED (63)
BIOS_SEL_PCIESATA2 (24)
M2_2_SEL (22,24)
BIOS_DIS_SW2 (24)
CPU_SKTOCC#_PCH
CPU_SKTOCC# (3,26)
SATA_PCIE_DET0 (14,23)
TP48
TP47
CNV_WR_CLK_DP (25)
CNV_WR_CLK_DN (25)
CNV_WR_0_DP (25)
CNV_WR_0_DN (25)
CNV_WR_1_DP (25)
CNV_WR_1_DN (25)
CNV_WT_CLK_DP (25)
CNV_WT_CLK_DN (25)
CNV_WT_0_DP (25)
CNV_WT_0_DN (25)
CNV_WT_1_DP (25)
CNV_WT_1_DN (25)
TP13
TP16
TP15
TP9
GPP_B2
WIFI_BTDIS#
(25) WIFI_BTDIS#
(35) SYSFAN5_MODE
(3,26) SIO_PROCHOT#
(29) CPUFAN1_FM
(30) PUMPFAN_FM
CPUFAN1_FM
PUMPFAN_FM
(33) SYSFAN3_MODE
(34) SYSFAN4_MODE
(18) CNV_BRI_DT
(25) CNV_BRI_DT_R
(25) CNV_BRI_RSP
(25) CNV_RGI_DT_R
(18) CNV_RGI_DT
(25) CNV_RGI_RSP
(18) GPP_J_9_CNV_MFUART2_TXD
CNV_BRI_DT
CNV_RGI_DT
GPPJ_RCOMP
TEST_SETUP_MENU
R694 10K/4 GPP_B2
CPUFAN1_FM R9 1K/4
PUMPFAN_FM R52 1K/4
R719 0R/4
R469 0R/4
R635 X_10K/4
R659 X_0R/4
R640 X_10K/4 GPP_I12 R639 10K/4
R629 X_10K/4 GPP_I13 R628 10K/4
R619 X_10K/4 GPP_I14 R618 10K/4
R475 10K/4
R476 X_10K/4
R481 10K/4
R486 10K/4
R480 X_10K/4
R1010 33R/4
R1011 33R/4
200R1%/4 R1153
200R1%/4 R970 1P8_RCOMP
200R1%/4 R623 3P3_RCOMP
R622 150R1%4
MICRO-STAR INT'L CO.,LTD
MS-7B51
Size Custom
Document Description
PCH-GPIO/RSVD
Rev 1.0
Date: Wednesday, May 23, 2018
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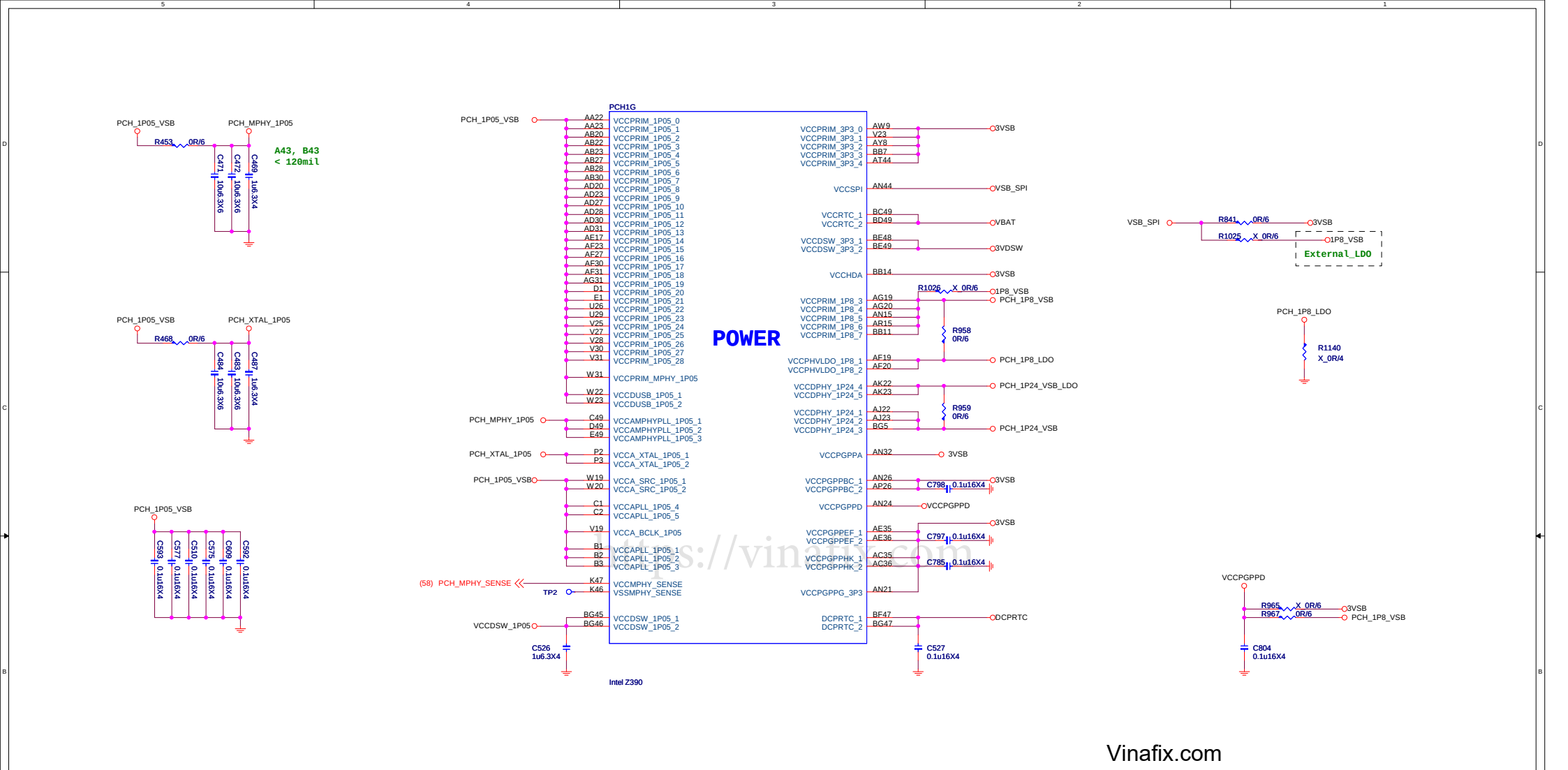

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MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: PCH-Power
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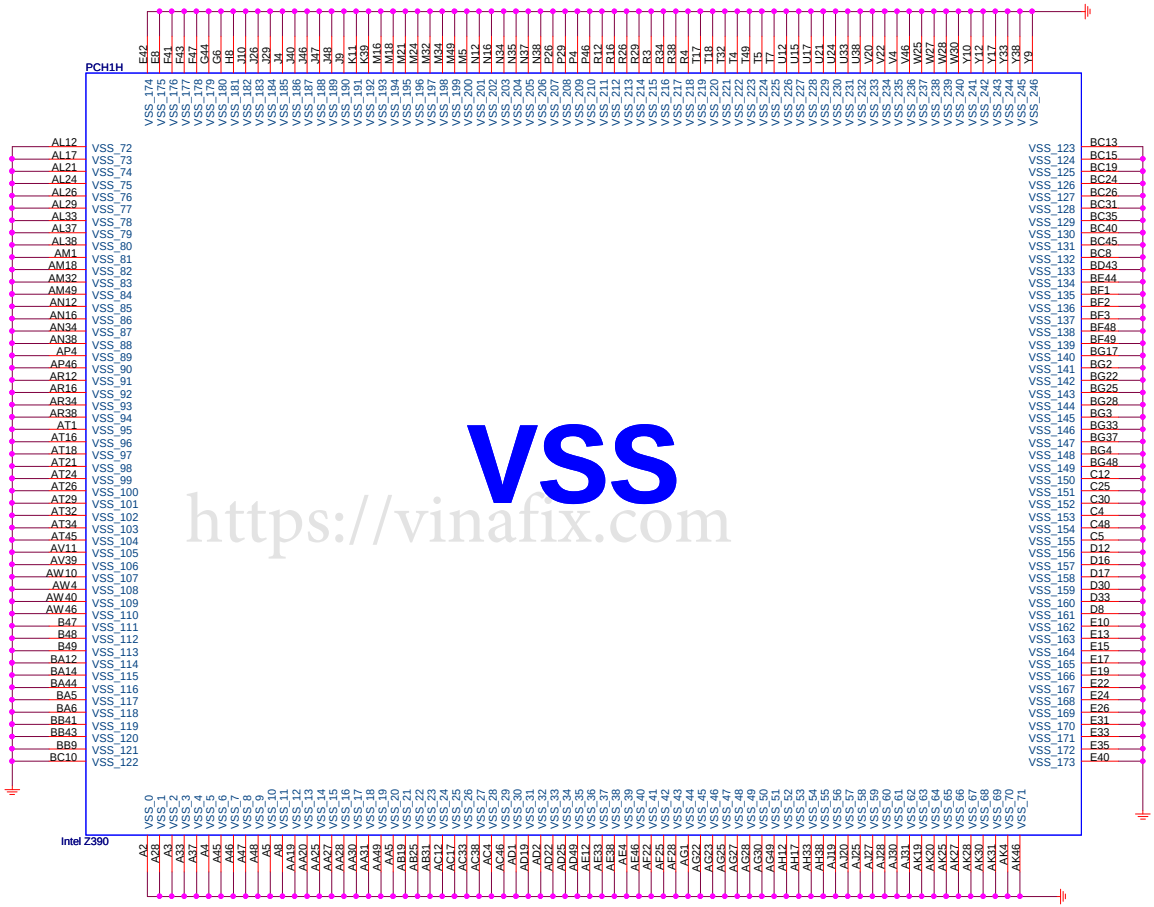
Date: Tuesday, May 22, 2018	Sheet 16 of 68



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MICRO-STAR INT'L CO.,LTD

MS-7B51

Size	Document Description	Rev
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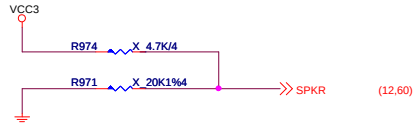
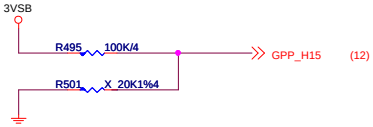
TOP Swap

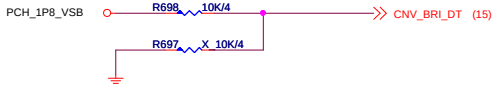


Internal Pull-down is disabled after PLTRST#

Reserved

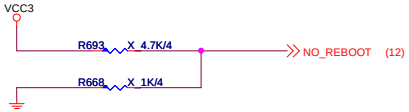


ESPI FLASH SHARING MODE



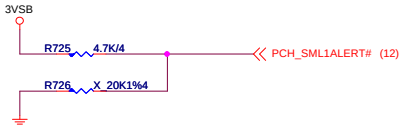
XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO
0 = 38.4/19.2MHZ

No Reboot

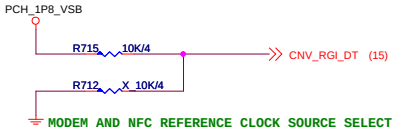


0 : DISABLE (Default)
1 : ENABLE

Reserved

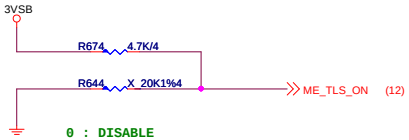


Modem Reference Clock Source Select



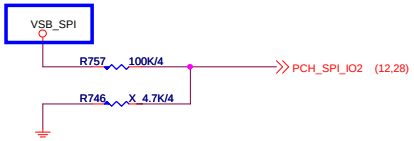
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT
1 = CLKIN_XTAL_LCP
0 = XTAL_IN (CNP AND LCP SHARE XTAL)

AMT and SBA with confidentiality

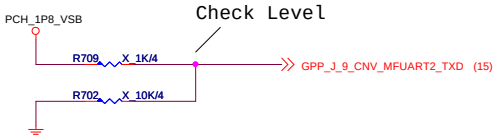


0 : DISABLE
1 : ENABLE (Default)

Reserved

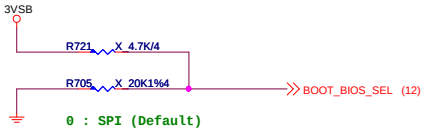


1.8V VCCPSPI



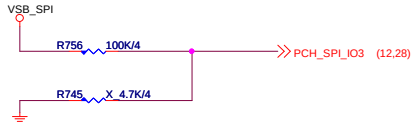
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCPSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

Boot BIOS

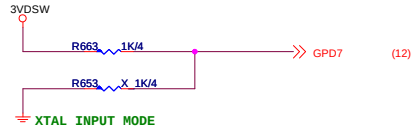


0 : SPI (Default)
1 : LPC

Reserved

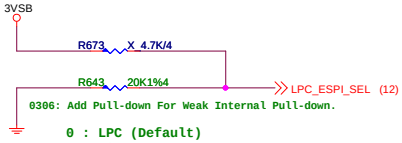


Reserved



XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD

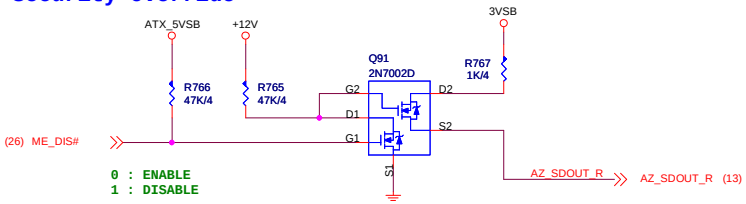
LPC eSPI Mode



0306: Add Pull-down For Weak Internal Pull-down.

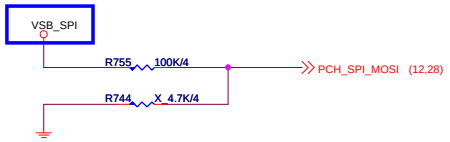
0 : LPC (Default)
1 : eSPI

Flash Descriptor Security Override

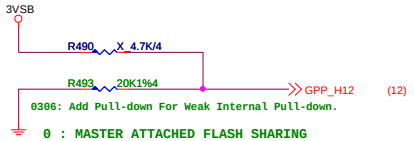


0 : ENABLE
1 : DISABLE

Reserved



ESPI FLASH SHARING MODE



0306: Add Pull-down For Weak Internal Pull-down.

0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

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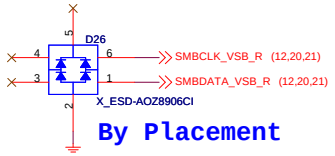
PCI_Express X16 Slot

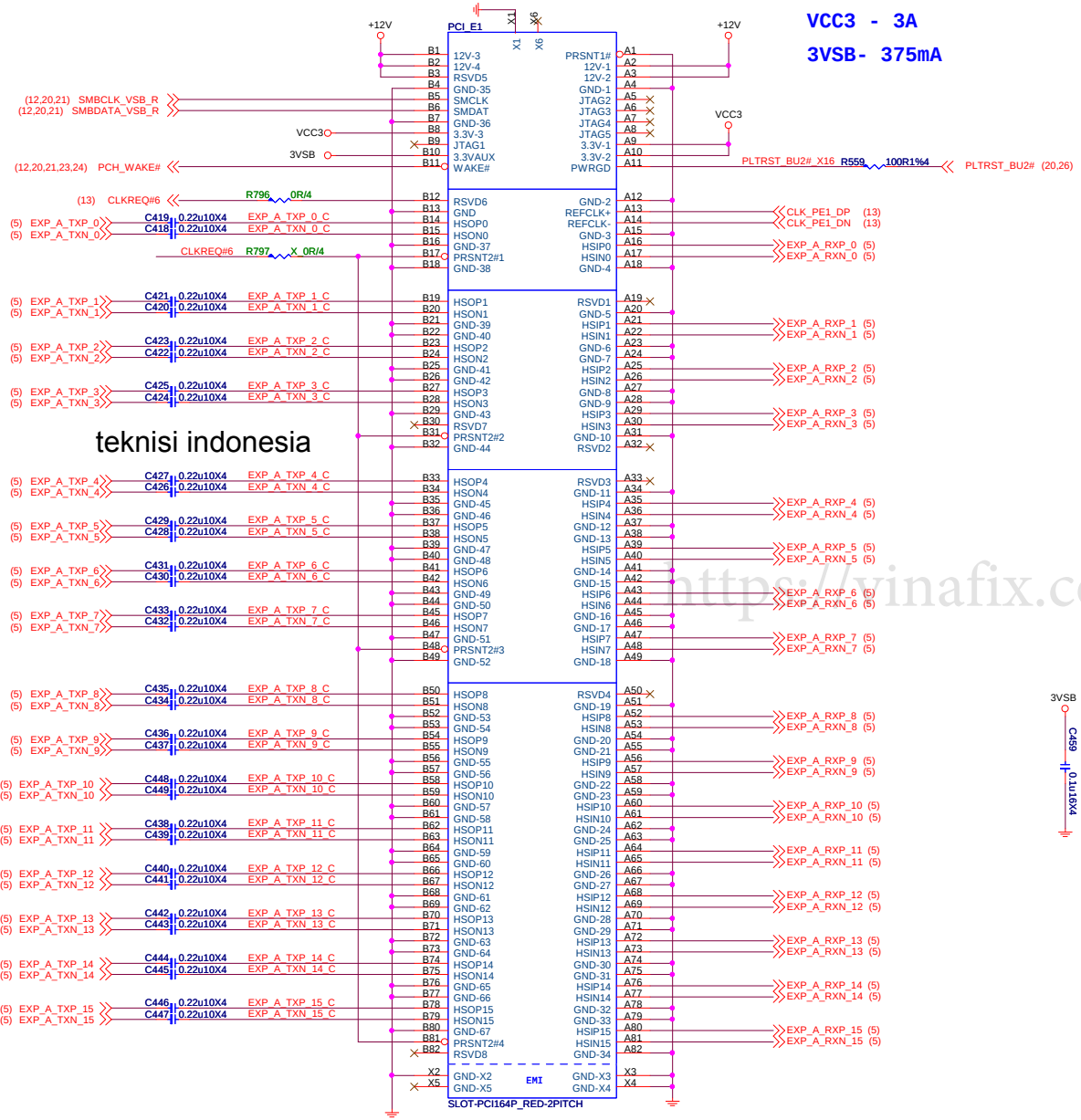
12V - 5.5A
VCC3 - 3A
3VSB- 375mA

SMBus ESD



By Placement

Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14



teknisi indonesia

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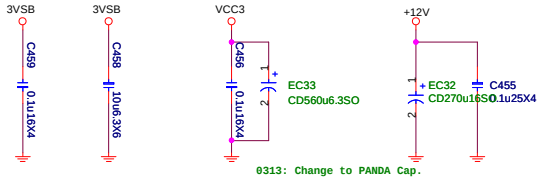

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Size: Custom	Document Description: PCIE SLOT (X16)	Rev: 1.0
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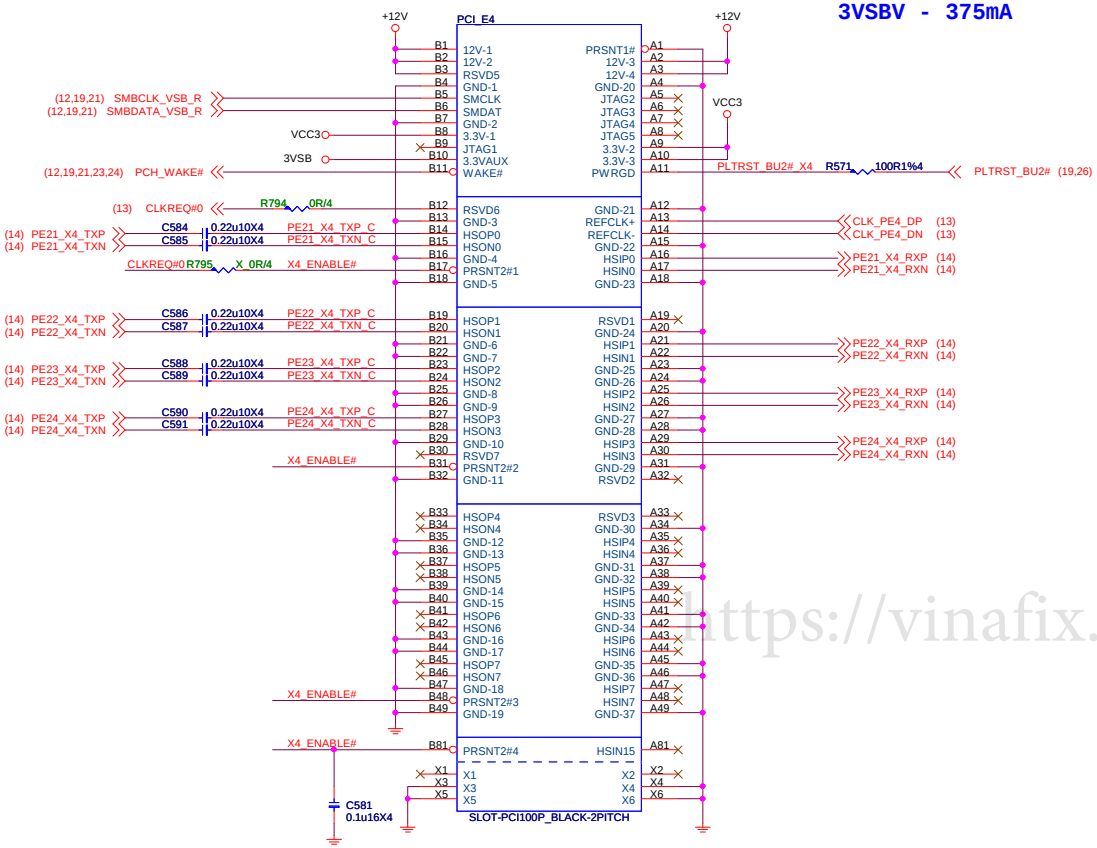
PCI_Express X4 Slot

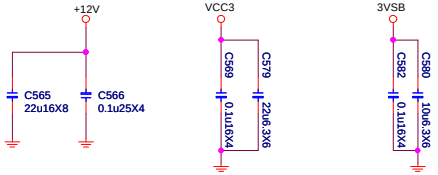
12V - 2.1A

VCC3 - 3A

3VSBV - 375mA



0522:Modify PCI_E4 Pin X3.X4.X5.X6 Connect to GND
Pin X1 X2 to Dummy



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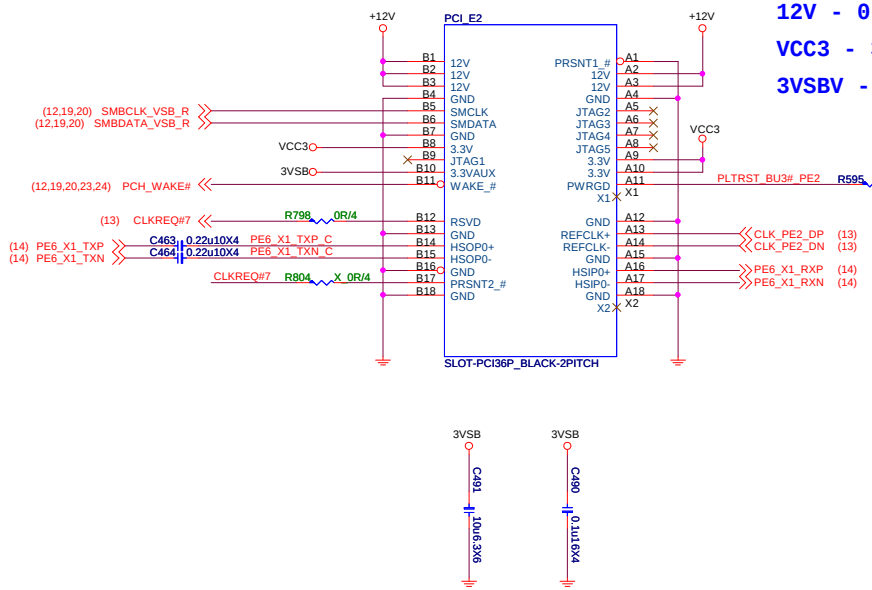
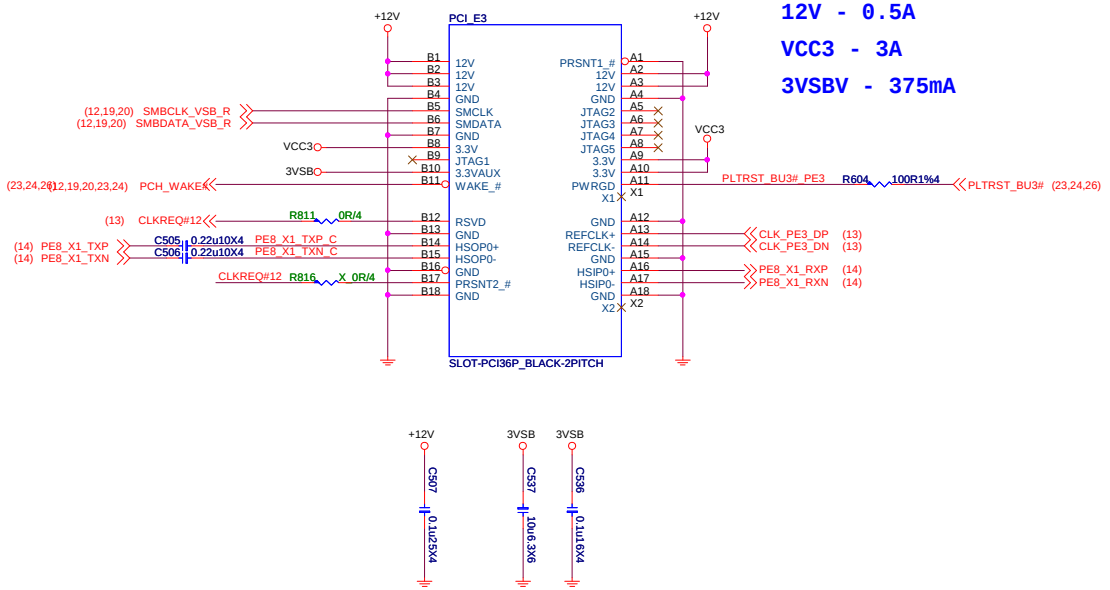
2016.08.25 Modify to N11-0360211-F02

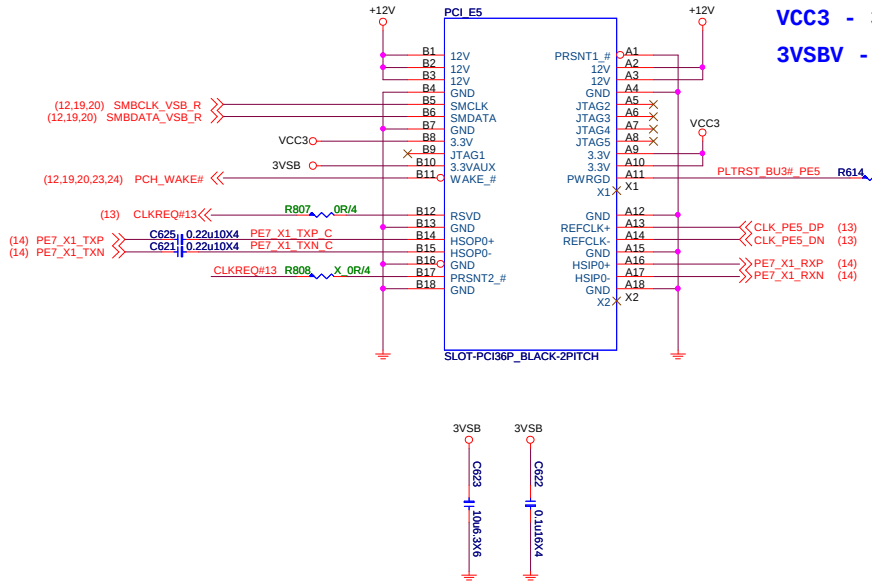


2016.08.25 Modify to N11-0360211-F02

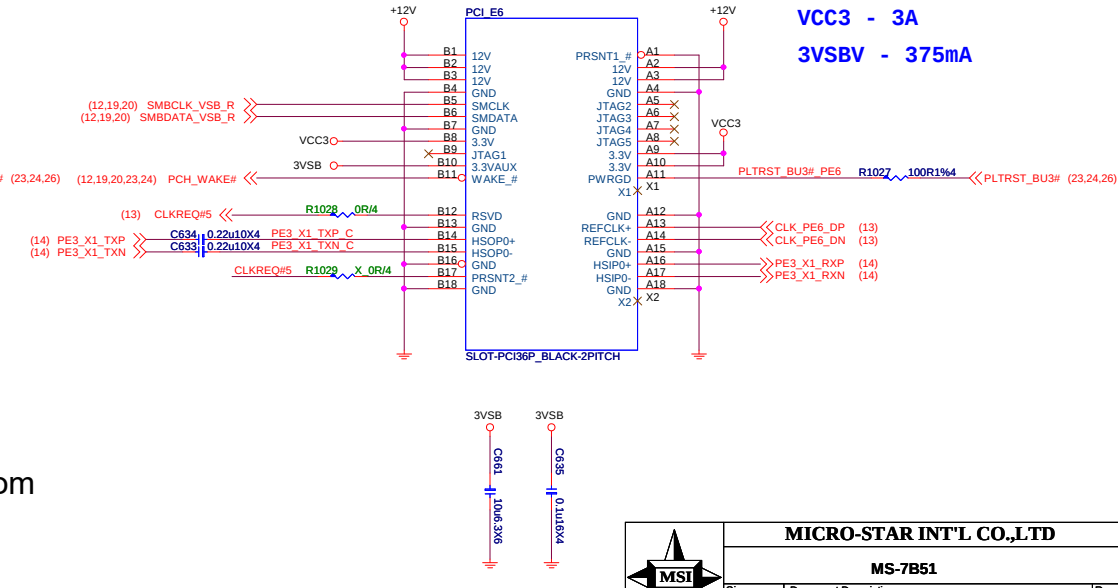


https://vinafix.com

2016.08.25 Modify to N11-0360211-F02



2016.08.25 Modify to N11-0360211-F02



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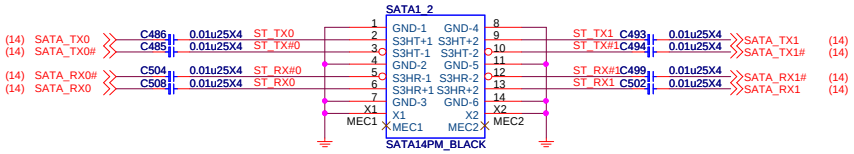
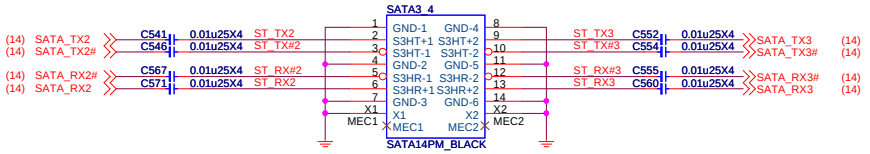
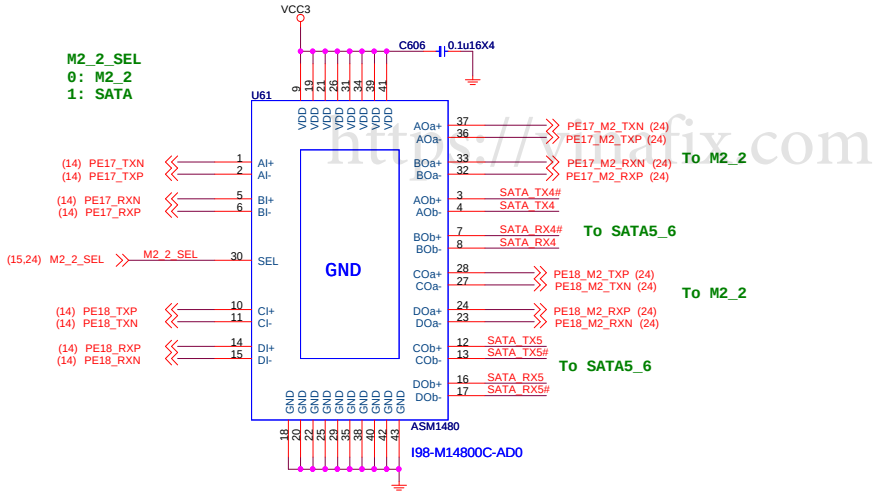
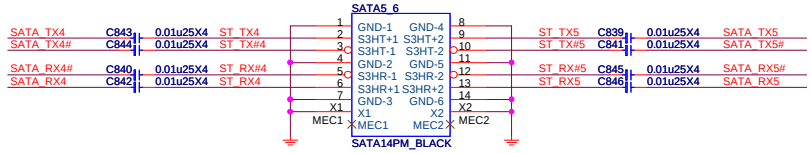
SATA Connector









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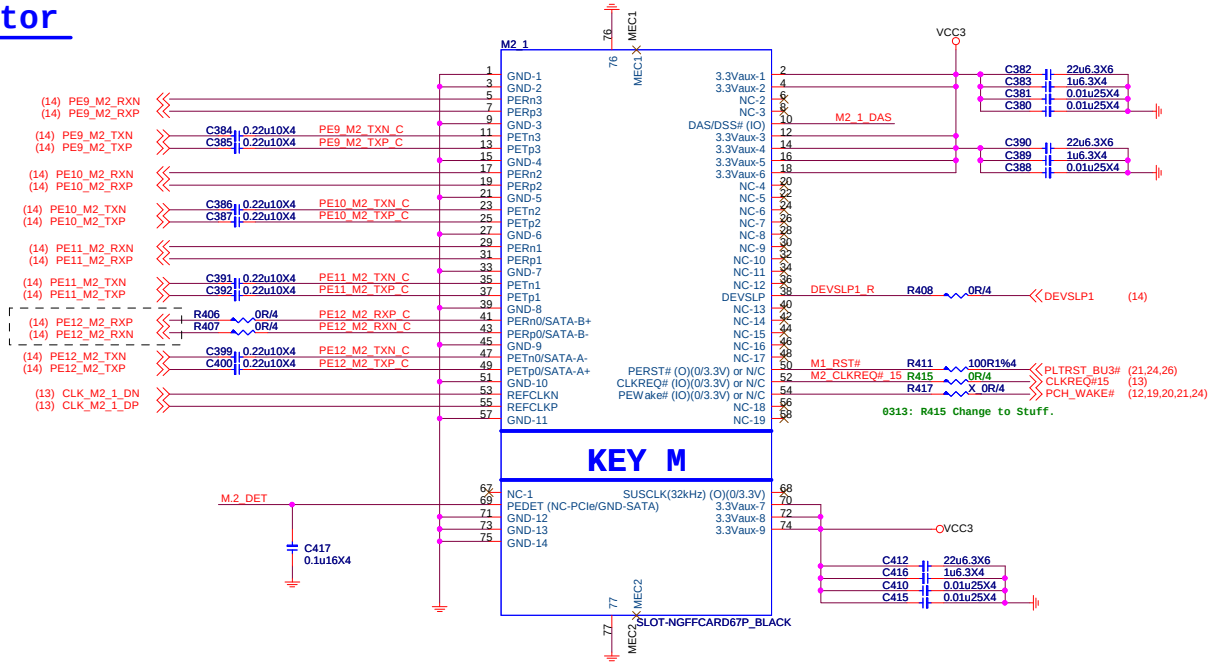
M.2 Connector



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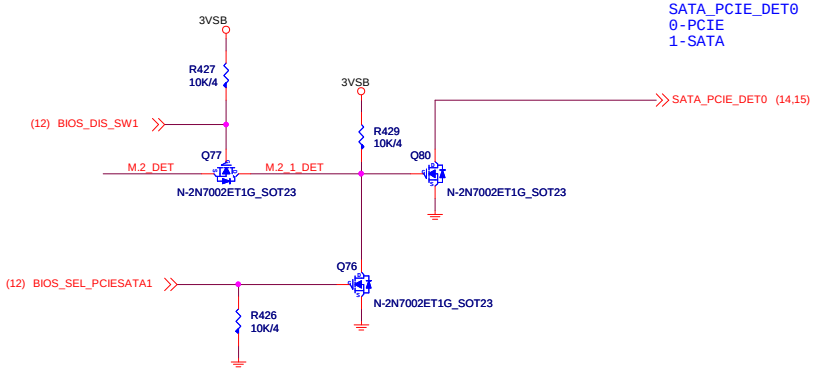
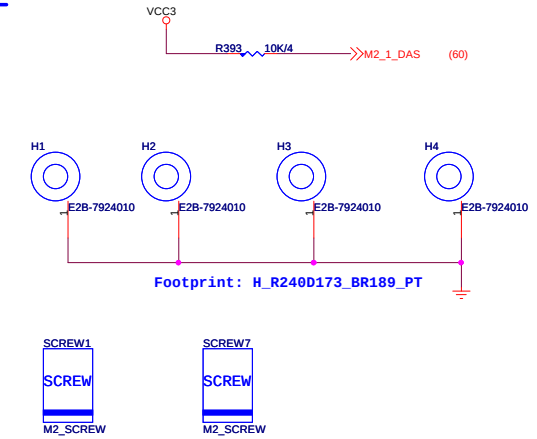


SATA_PCIE_DET0
0-PCIE
1-SATA

BIOS_MODE

BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

22 * 110



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Size	Document Description	Rev
Custom	M.2-SLOT1	1.0

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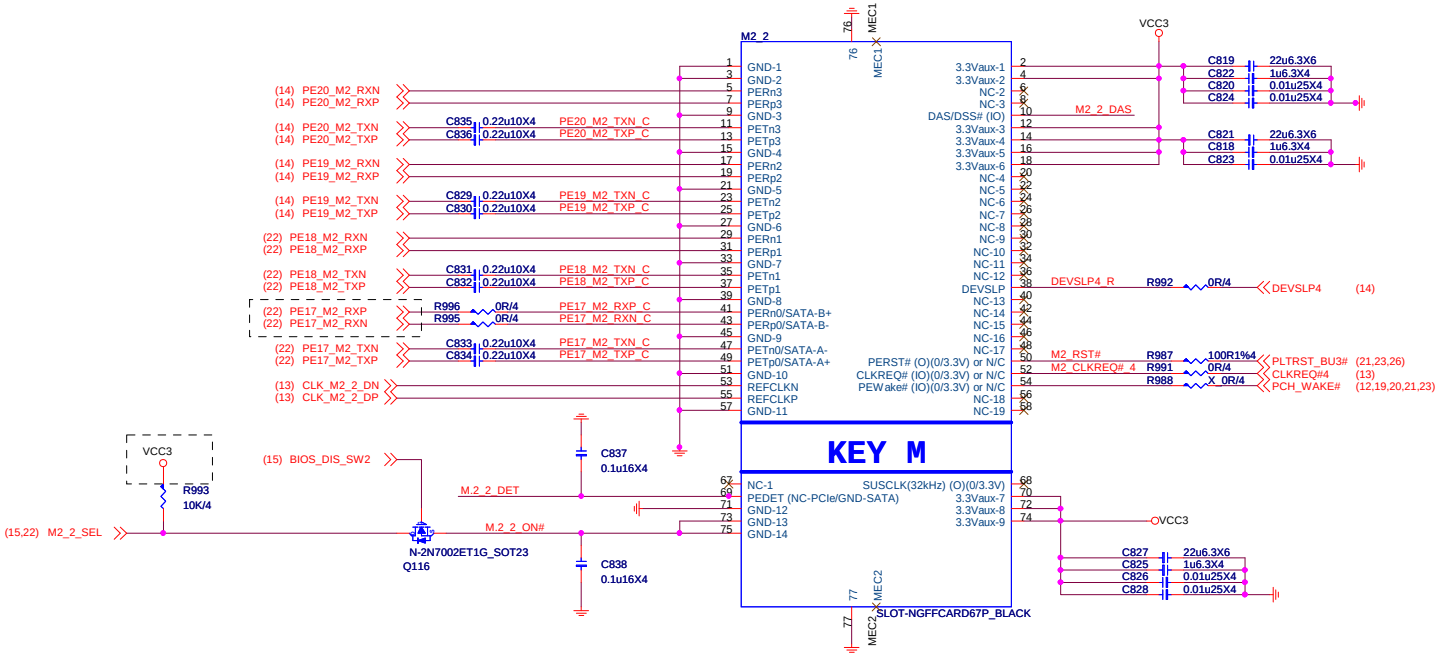

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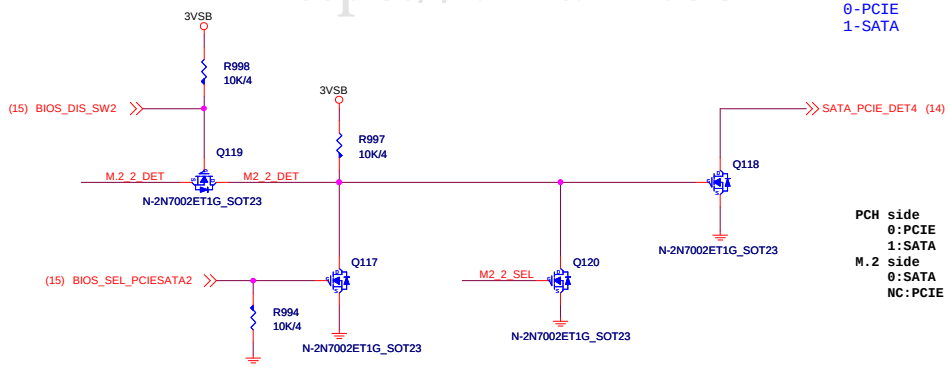
SATA_PCIE_DET4
0-PCIE
1-SATA



BIOS_MODE

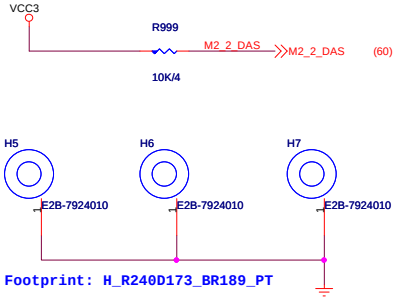
To Switch SATA5

To Switch SATA5

GPP_G7 GPP_G6 GPP_G5

BIOS_DIS_SW2	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*	*SATA_PCIE_DET4*
GPI(1)	*GPI(1)*	*GPI(0)*	*AUTO*	
0	*1*	*0*	*SATA5*	*1*
0	*0*	*1*	*M2-SATA*	*1*
0	*0*	*0*	*M2-PCIE*	*0*

22 * 80



SCREW2 SCREW6

SCREW SCREW

M2_SCREW M2_SCREW

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Custom	M.2-SLOT2	0A

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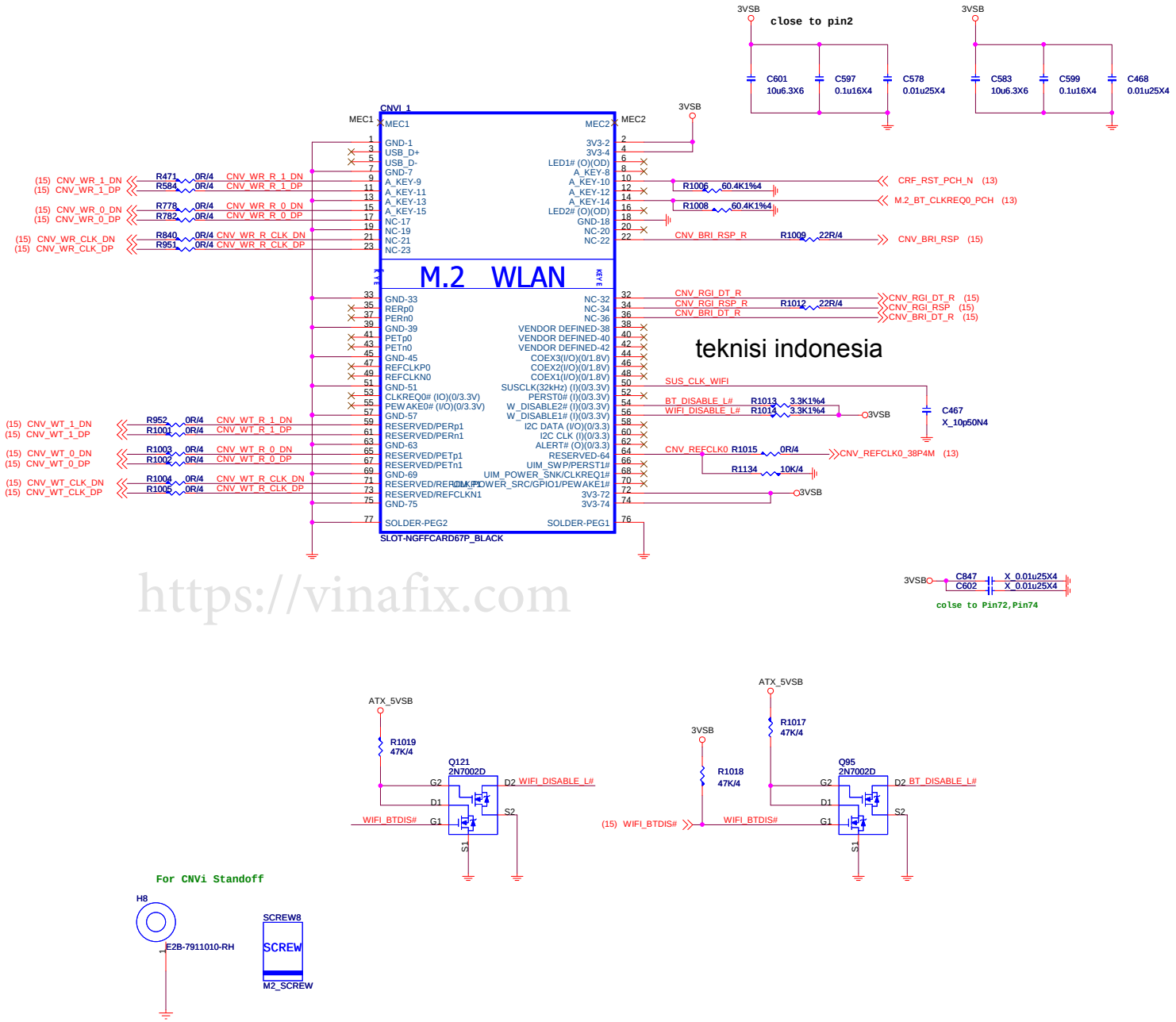

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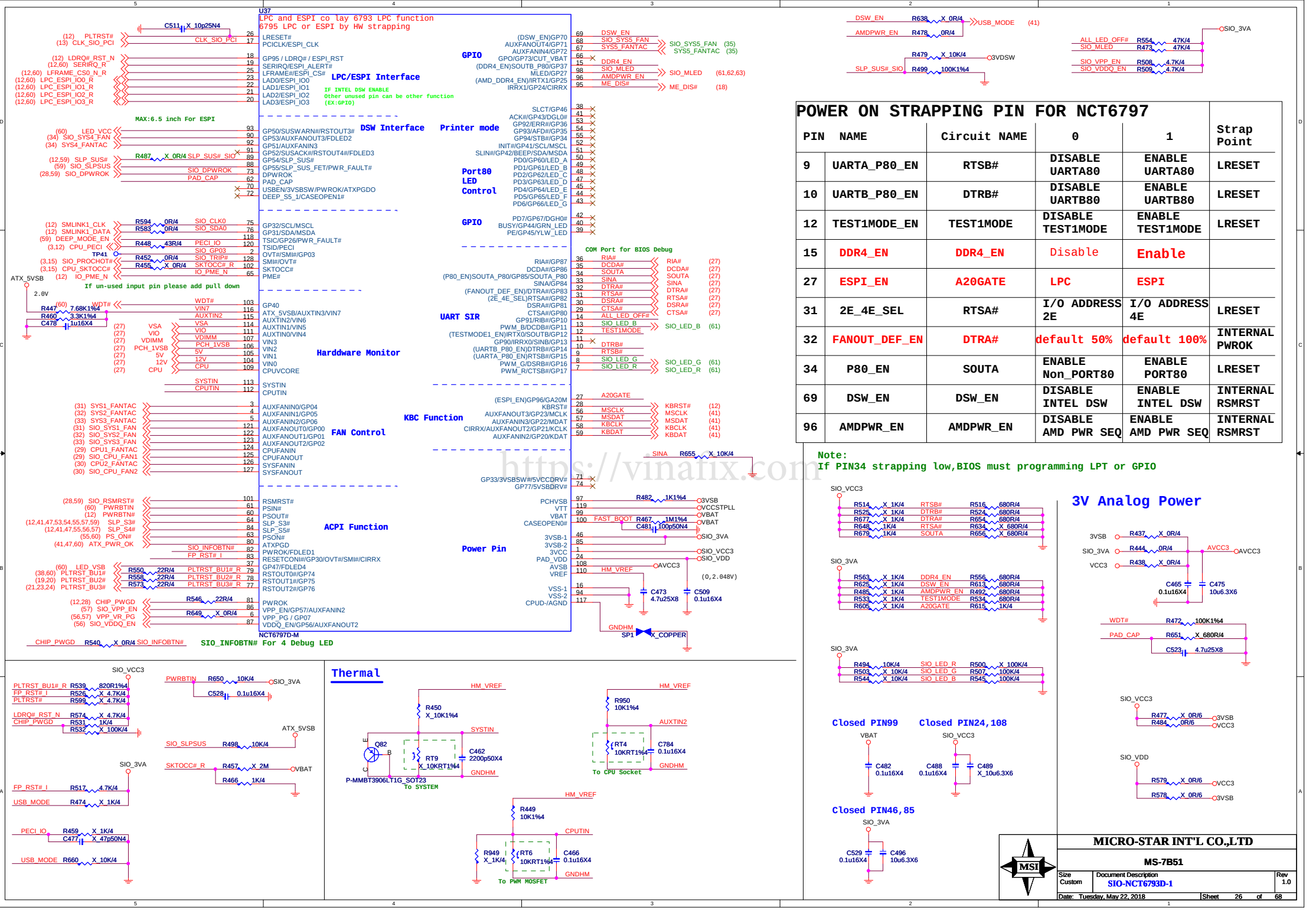

POWER ON STRAPPING PIN FOR NCT6797

PIN	NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	A20GATE	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

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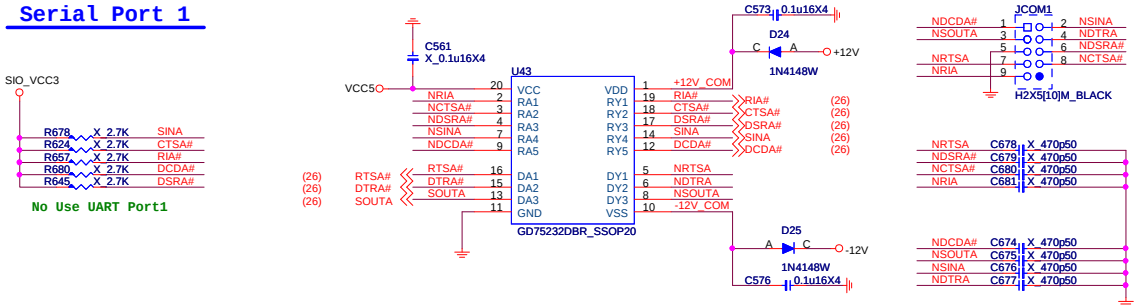
Serial Port 1



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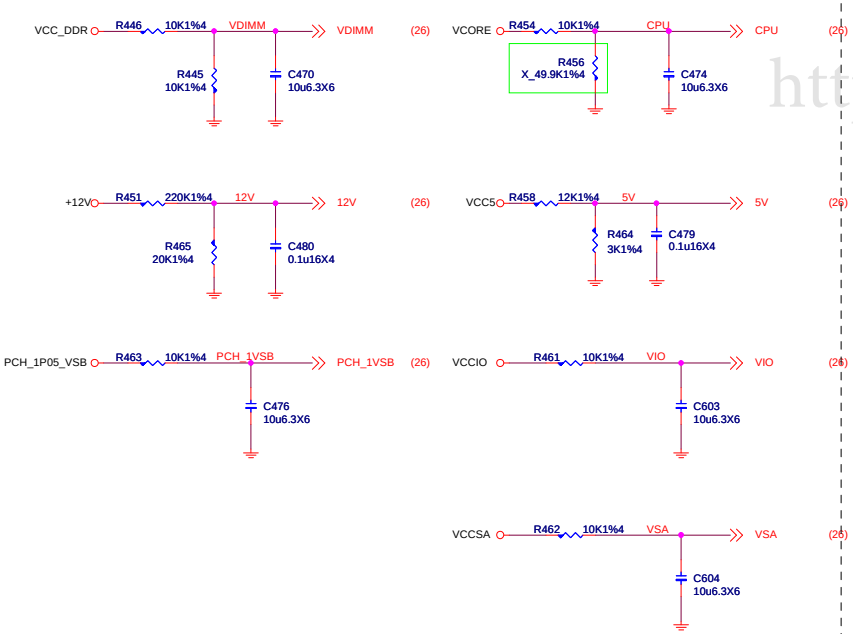
HW Monitor - Voltage

SIO HM Voltage Over 2V will Not Detect



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0517: Delete Redundant Components

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MS-7B51		
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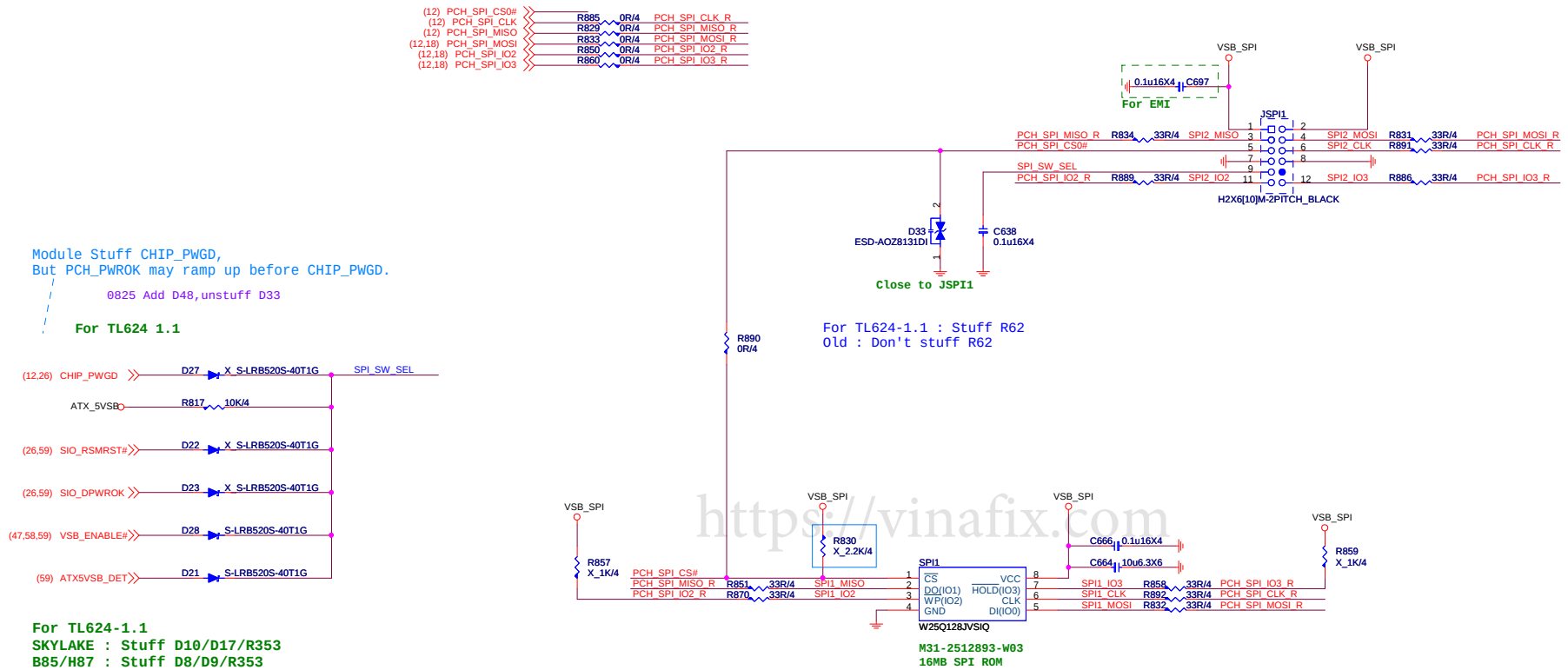
BIOS



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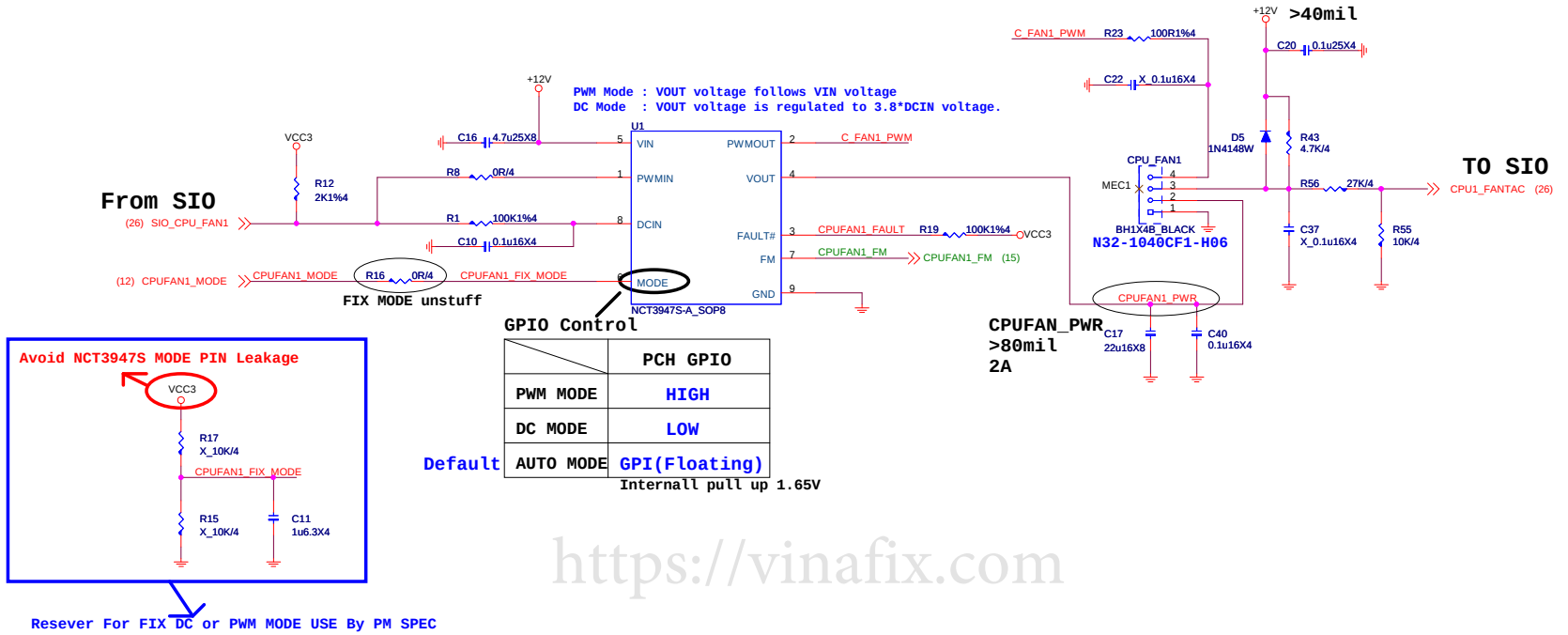
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



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MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: CPU FAN1 — Rev: 1.0
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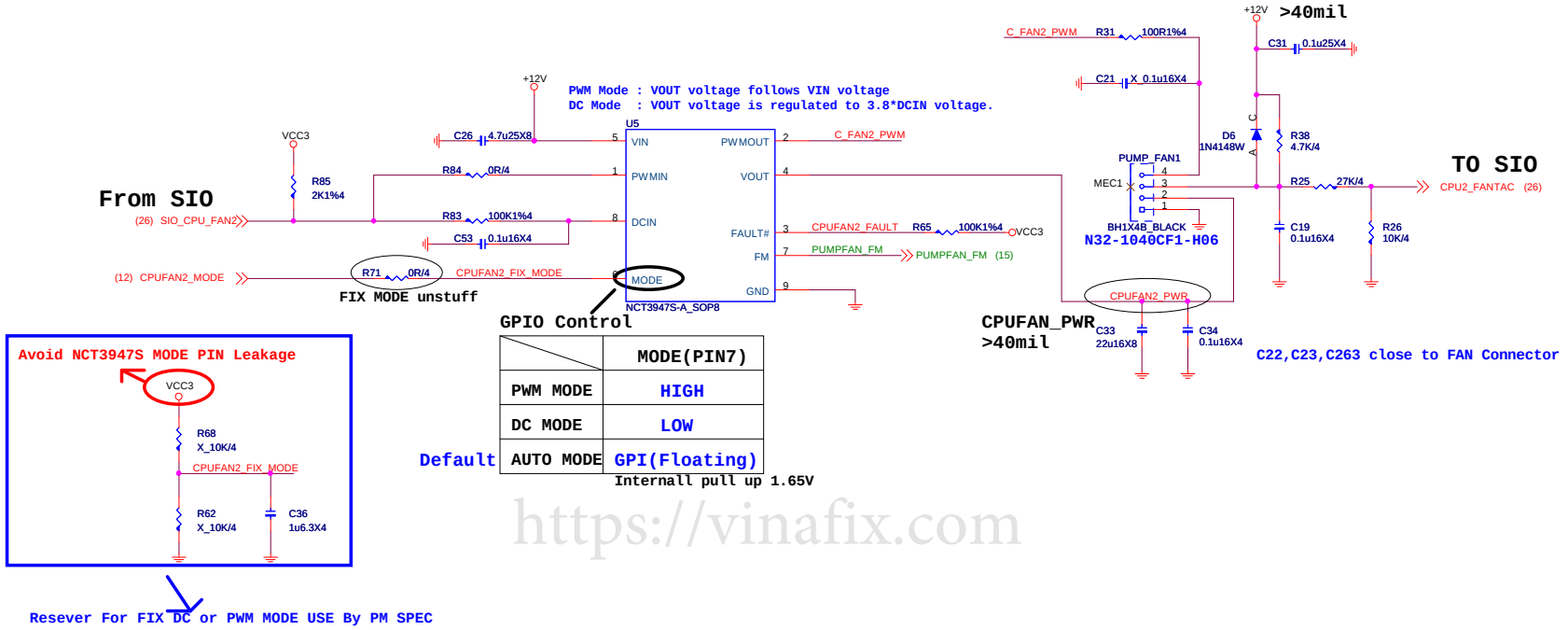
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

Resever For FIX DC or PWM MODE USE By PM SPEC

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Size: Custom | Document Description: PUMP_FAN1 | Rev: 1.0

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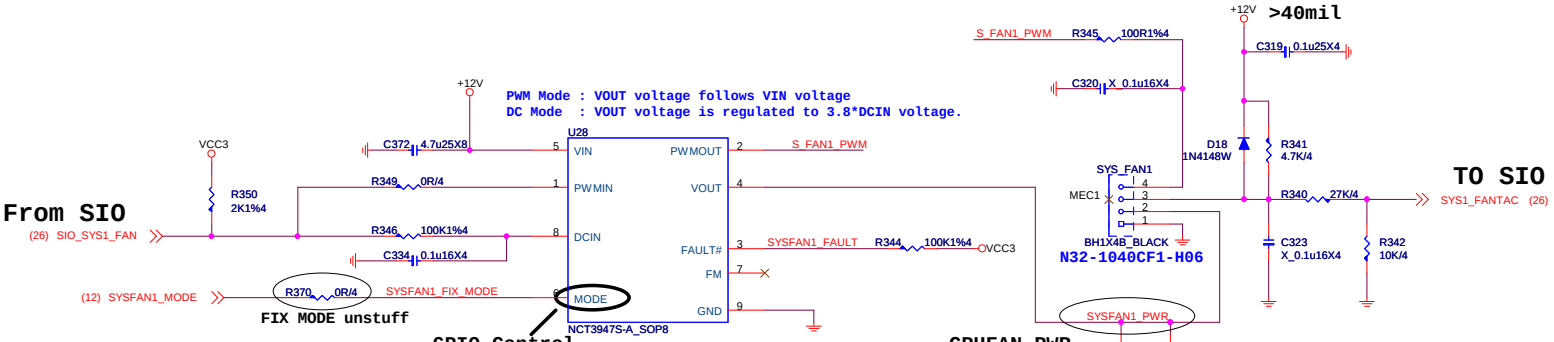
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

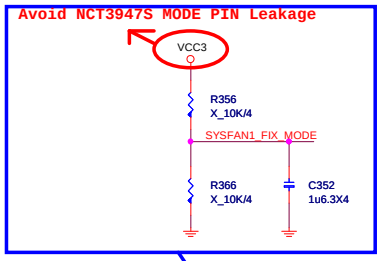
1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

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Size: Custom | Document Description: SYSTEM FAN1 | Rev: 1.0

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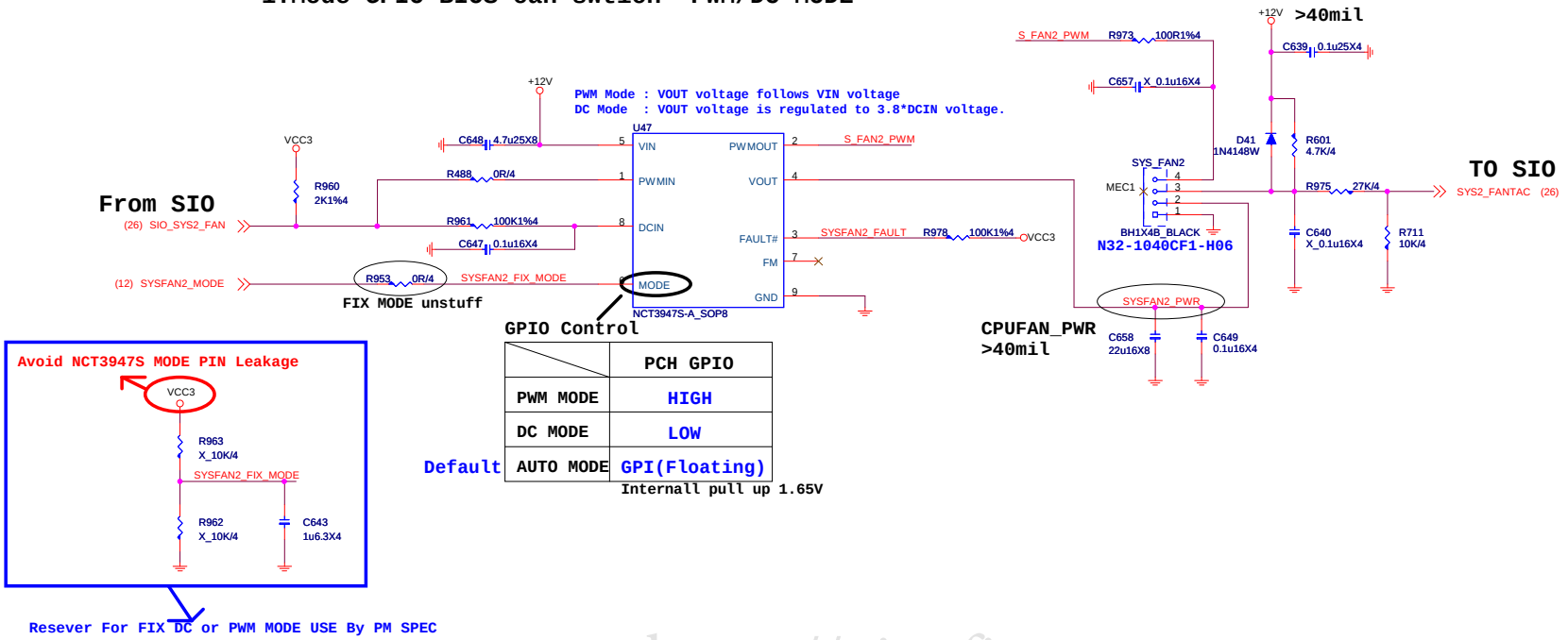
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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MS-7B51	
Size: Custom	Document Description: SYSTEM FAN2 — Rev: 1.0
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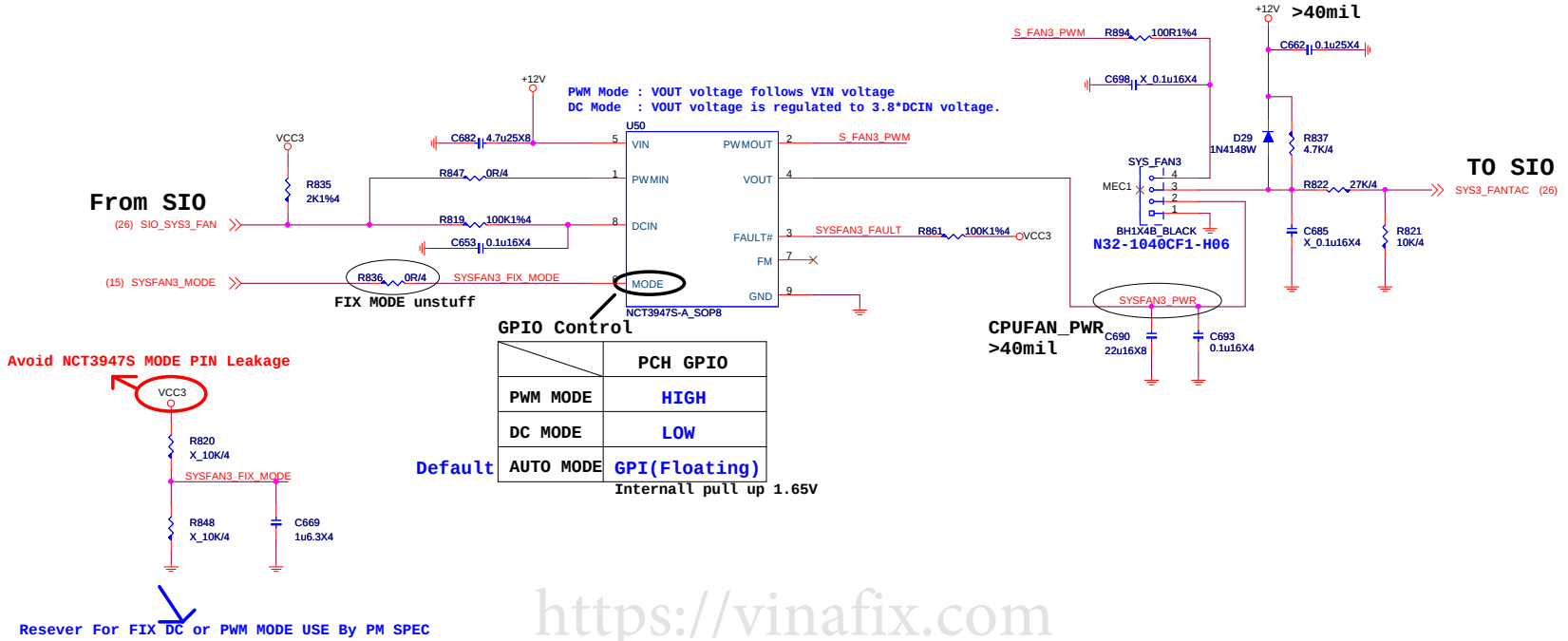
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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MS-7B51	
Size: Custom	Document Description: SYSTEM FAN3
Rev: 1.0	
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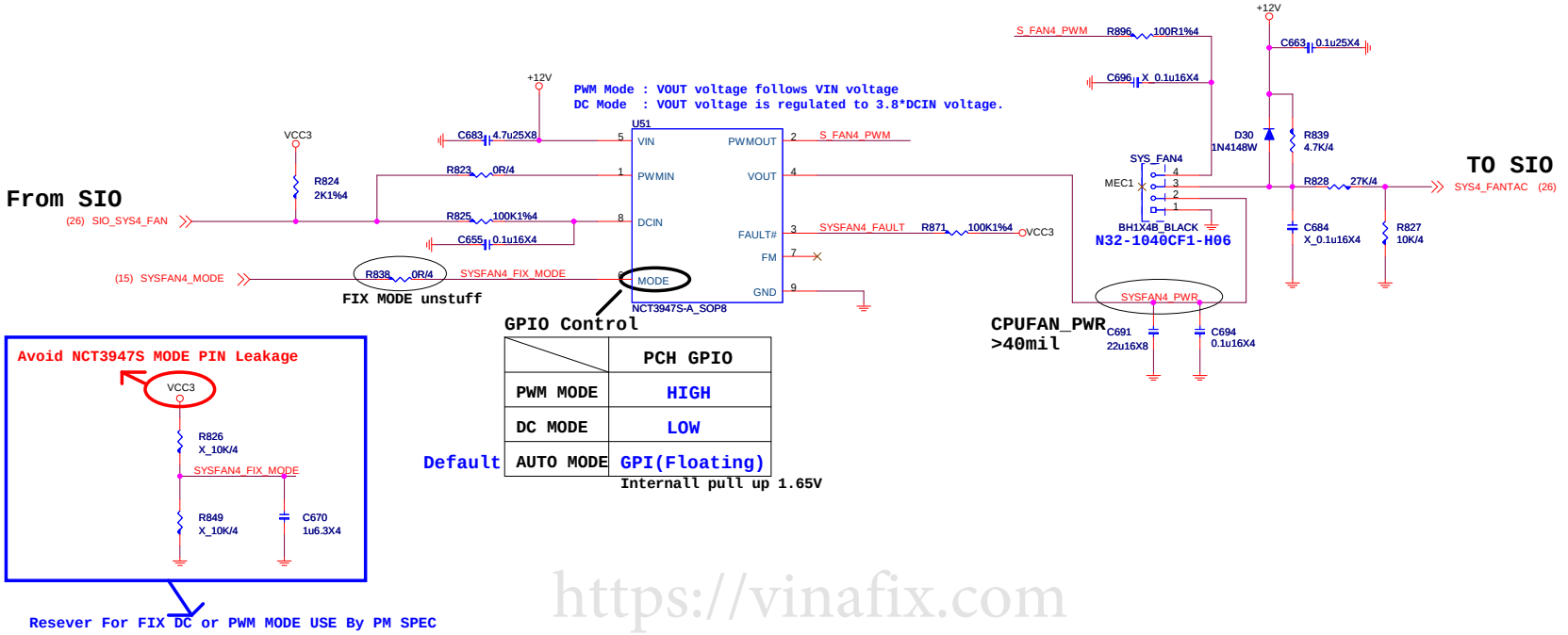
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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Rev: 1.0	
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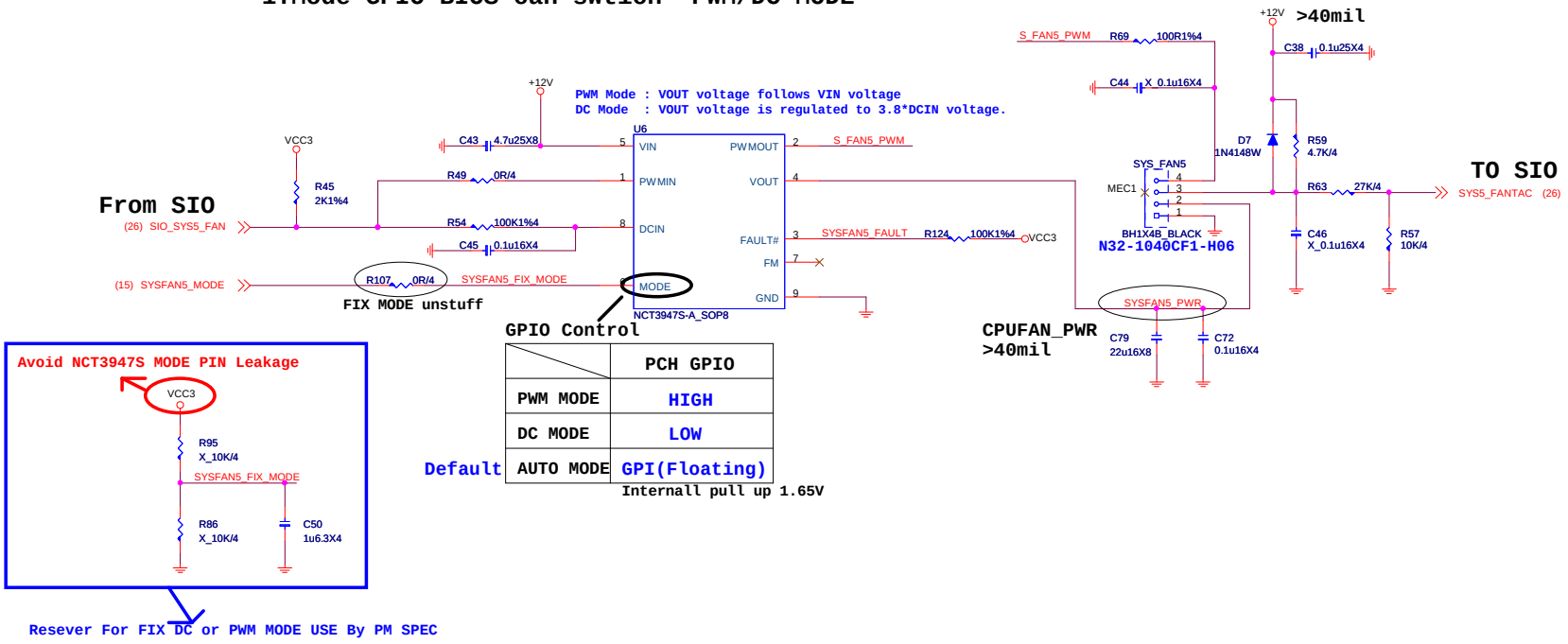
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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MS-7B51	
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Rev: 1.0	
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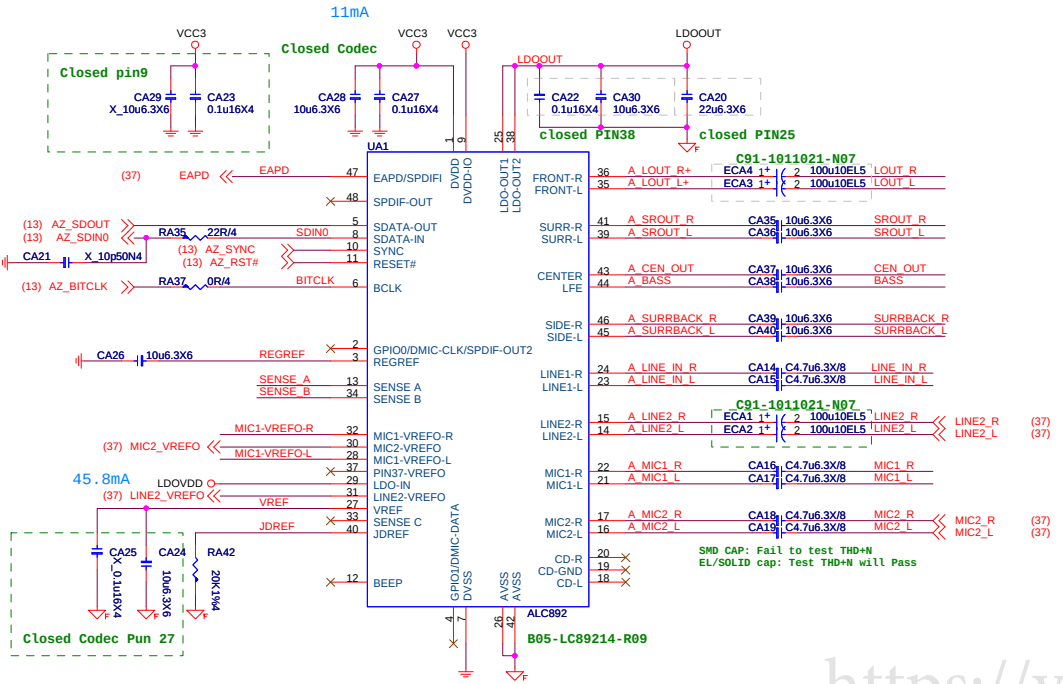
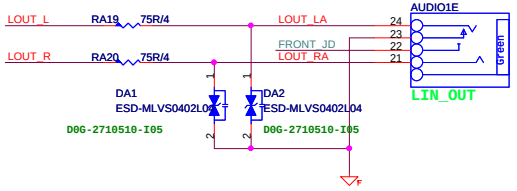
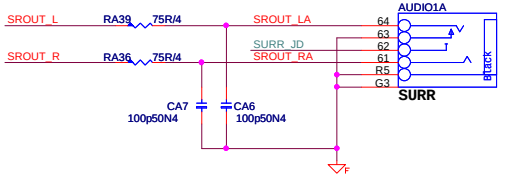
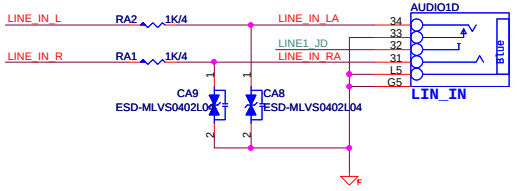
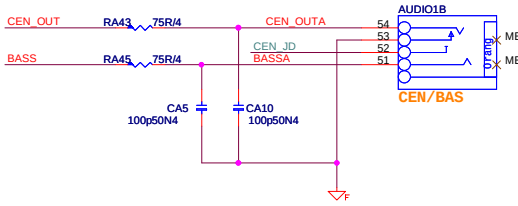
ALC892

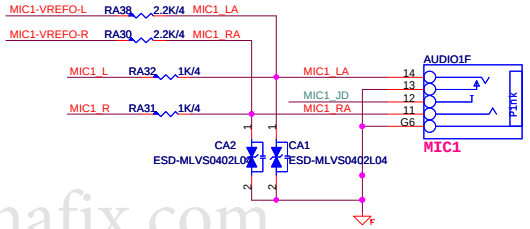


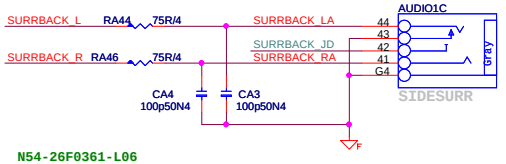


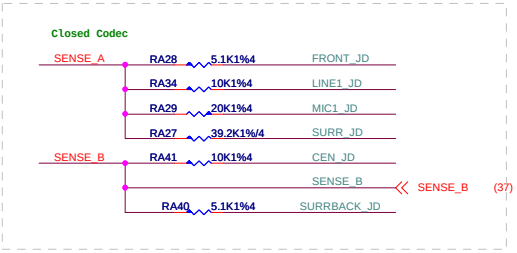


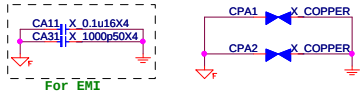


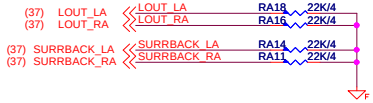


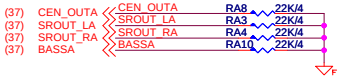


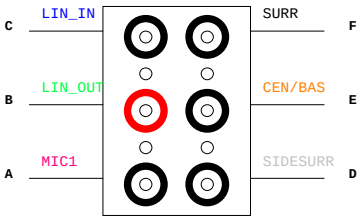


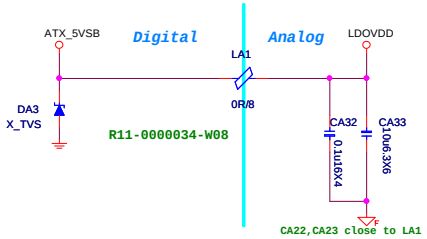












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MICRO-STAR INT'L CO.,LTD

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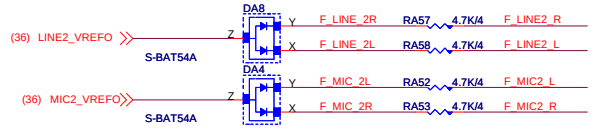
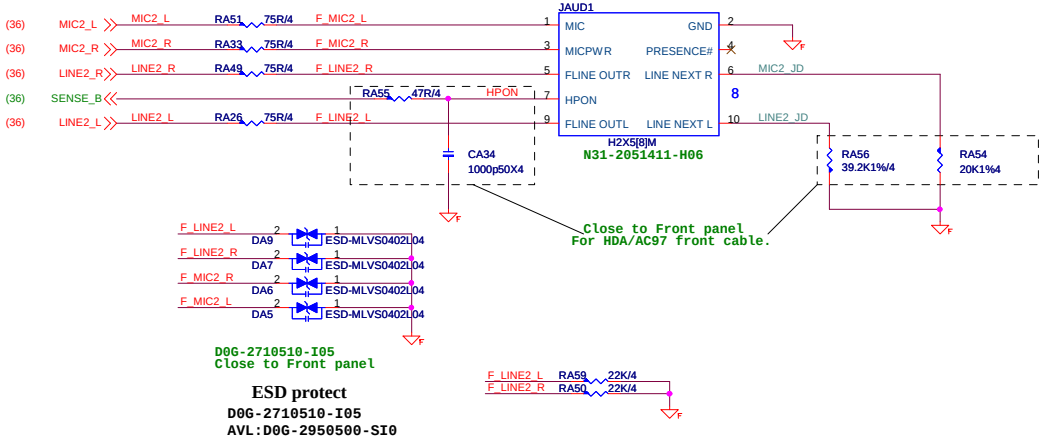
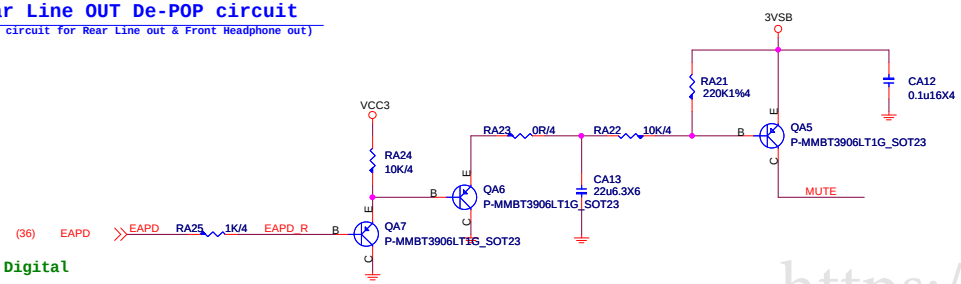




Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)



Digital

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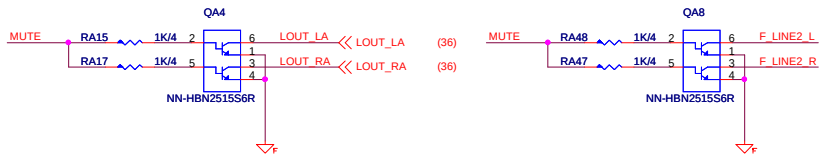
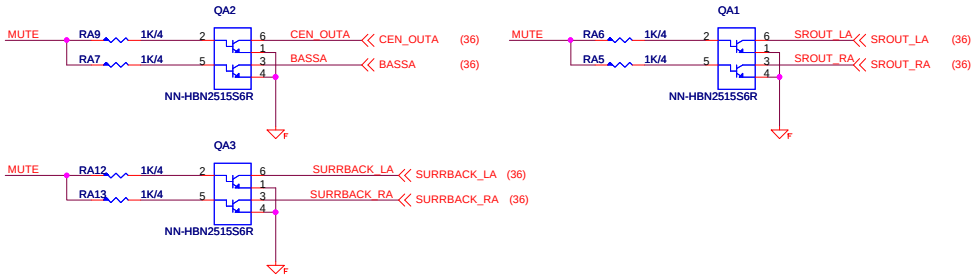
Analog



(Add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5,CA6, CA7, CA9,to TVS)



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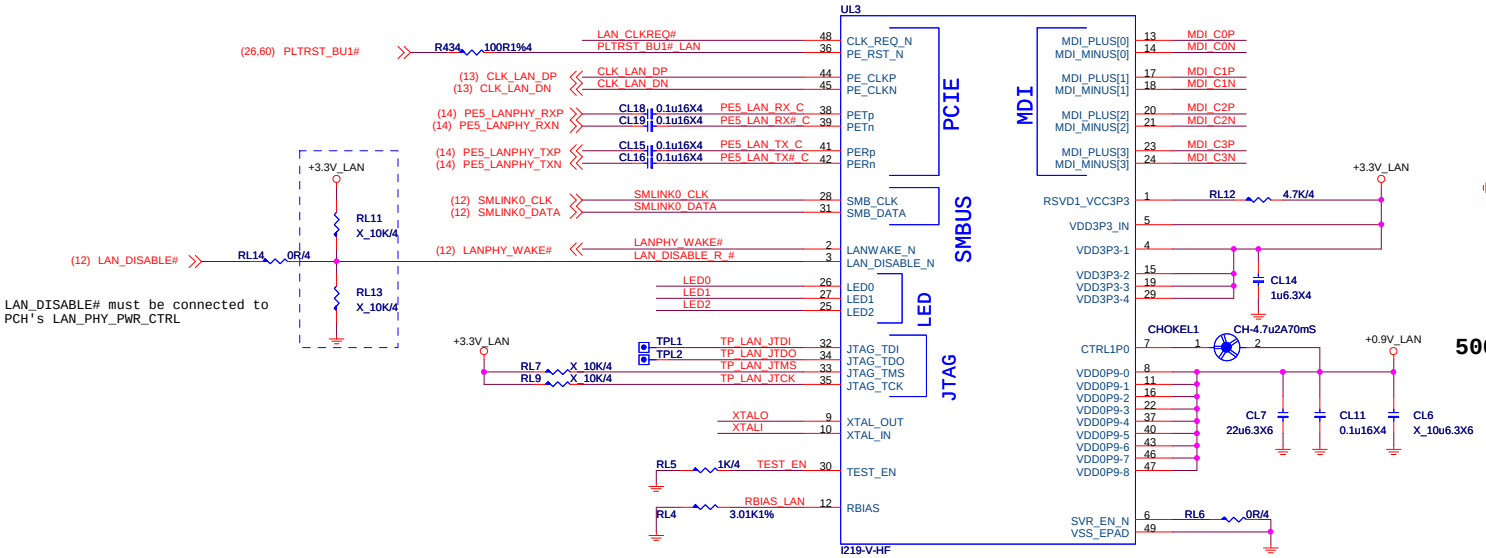
Intel Lan- i219

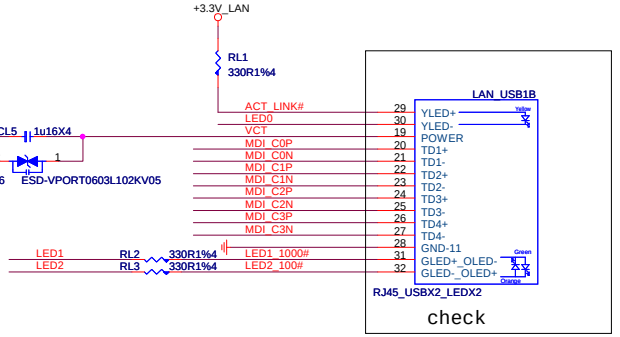
LAN Connector

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

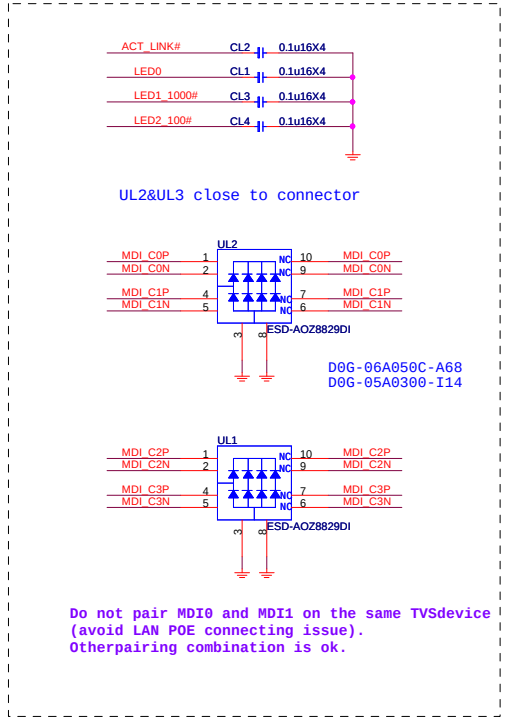


LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

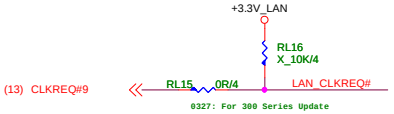
500mA

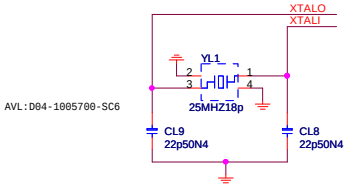


For EMI



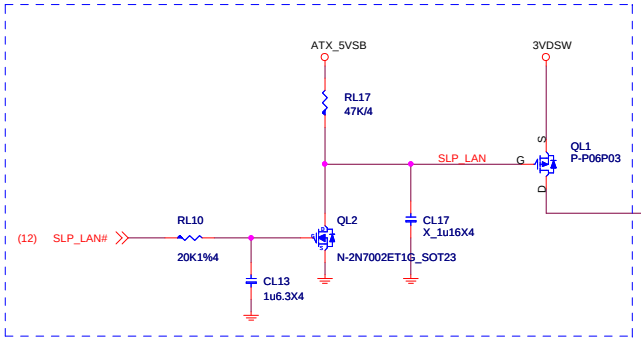
PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

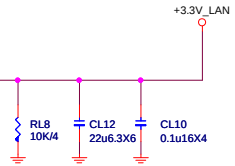




The 10Kohm pull-up resistor (RL18) of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.





+3.3V_LAN
I218:132mA
I219:542mW

Note:These caps closed to PHY

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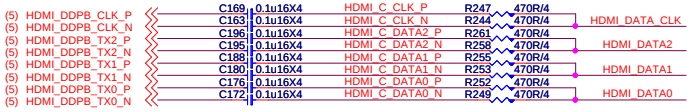
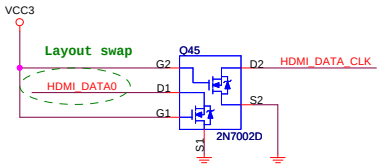
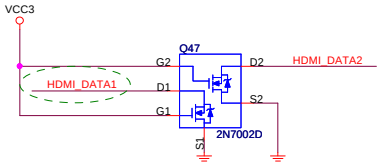
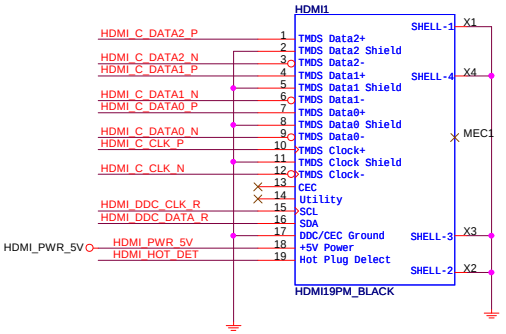
HDMI 1.4b

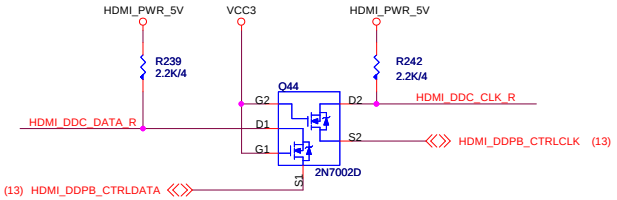
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

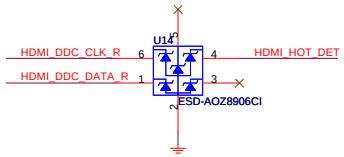


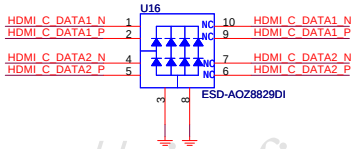


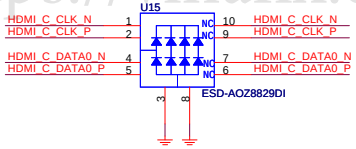


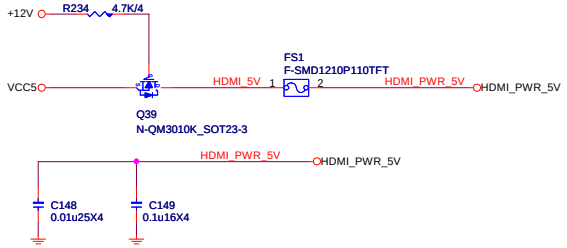












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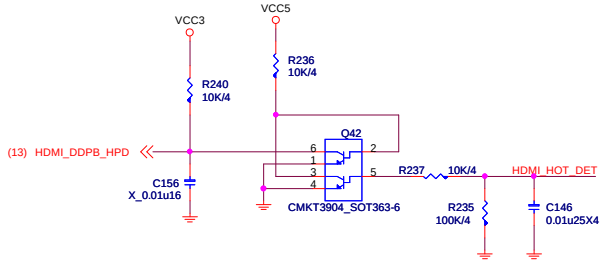
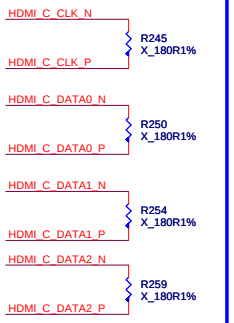
Hot Plug

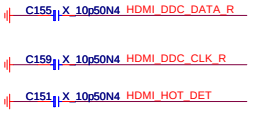


For EMI



0B版可以考慮是否刪除這4顆電阻

For EMI



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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

(5) DVI_DDPC_CLK_P
(5) DVI_DDPC_CLK_N
(5) DVI_DDPC_TXP0
(5) DVI_DDPC_TXN0
(5) DVI_DDPC_TXP1
(5) DVI_DDPC_TXN1
(5) DVI_DDPC_TXP2
(5) DVI_DDPC_TXN2

C89 0.1u16X4 DVI_C_CLK_P R139 470R/4
C91 0.1u16X4 DVI_C_CLK_N R131 470R/4
C95 0.1u16X4 DVI_C_DATA0_P R150 470R/4
C91 0.1u16X4 DVI_C_DATA0_N R143 470R/4
C104 0.1u16X4 DVI_C_DATA1_P R163 470R/4
C98 0.1u16X4 DVI_C_DATA1_N R157 470R/4
C114 0.1u16X4 DVI_C_DATA2_P R174 470R/4
C111 0.1u16X4 DVI_C_DATA2_N R165 470R/4

VCC3
Q113
N-2N7002ET1G_SOT23

VCC5 D10 S-1N5817 DVI_5V FSV2 F-SMD1210P110TFT DVI_PWR_5V
CV27 0.1u16X4
EMI

DVI1
DVI_C_DATA2_N DVI_C_DATA2_P DVI_DDC_CLK_R DVI_DDC_DATA_R DVI_C_DATA1_N DVI_C_DATA1_P DVI_HOT_DET DVI_C_DATA0_N DVI_C_DATA0_P DVI_C_CLK_P DVI_C_CLK_N
Shell-1 DATA2 DATA2 SHIELD24 DATA4 DATA4 DDCCLK DDCDATA NC DATA1 DATA1 SHIELD13 DATA3 DATA3 VCC5 GND5 HPDET DATA0 DATA0 SHIELD05 DATA5 DATA5 SHIELDCLK CLK CLK Shell-2 Shell-3 Shell-4 Shell-5 Shell-6
DVI24P_BLACK

U26 AVL:D0G-05A050C-005
D0G-06A050C-A68

U9
ESD-AOZ8829DI
DVI_C_DATA0_P DVI_C_DATA0_N DVI_C_CLK_P DVI_C_CLK_N
DVI_C_DATA0_P DVI_C_DATA0_N DVI_C_CLK_P DVI_C_CLK_N

U27 AVL:D0G-05A050C-005
D0G-06A050C-A68

U11
ESD-AOZ8829DI
DVI_C_DATA1_N DVI_C_DATA1_P DVI_C_DATA2_N DVI_C_DATA2_P
DVI_C_DATA1_N DVI_C_DATA1_P DVI_C_DATA2_N DVI_C_DATA2_P

DVI_PWR_5V VCC3 DVI_PWR_5V
R221 2.2K/4 R216 2.2K/4
Q34
DVI_DDC_CLK_R DVI_DDC_DATA_R
DVI_DDPC_CTRLDATA (13)
2N7002D
(13) DVI_DDPC_CTRLCLK

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For EMI
DVI_C_DATA0_N DVI_C_DATA0_P R148 X_243R1%
DVI_C_DATA1_N DVI_C_DATA1_P R159 X_243R1%
DVI_C_CLK_N DVI_C_CLK_P R137 X_243R1%
DVI_C_DATA2_N DVI_C_DATA2_P R172 X_243R1%

HPD
DVI_PWR_5V
VCC3
R227 10K/4
R228 10K/4
(13) DVI_DDPC_HPD
Q35
DVI_HOT_DET_R R223 10K/4 DVI_HOT_DET
C141 X_0.01u16
CMKT3904_SOT363-6
R224 100K/4

EMI
DVI_HOT_DET
DVI_DDC_CLK_R
DVI_DDC_DATA_R
C133 X_10p50N4 C135 X_10p50N4 C136 X_10p50N4

D9
DVI_DDC_CLK_R DVI_HOT_DET DVI_DDC_DATA_R
ESD-AOZ8906CI

MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description DVI Connector
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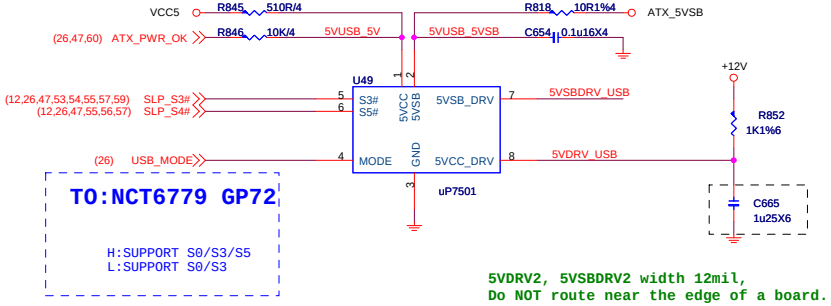
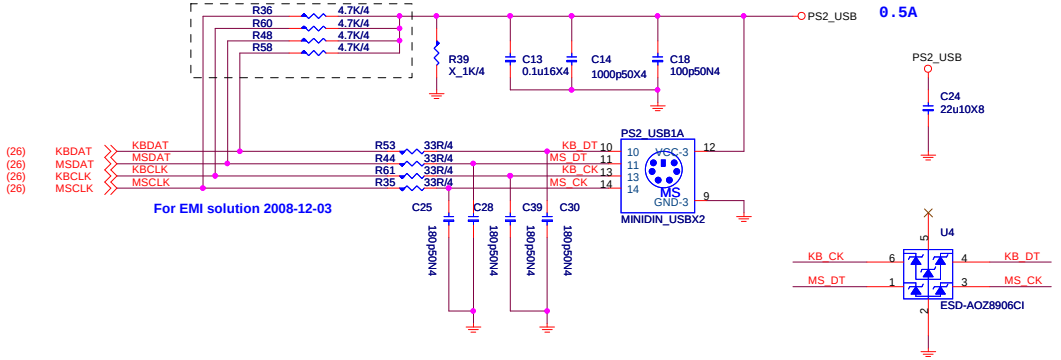
USB Power

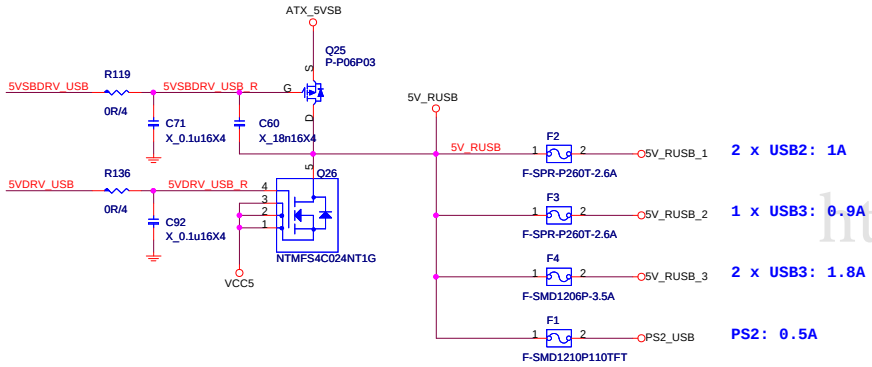


5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

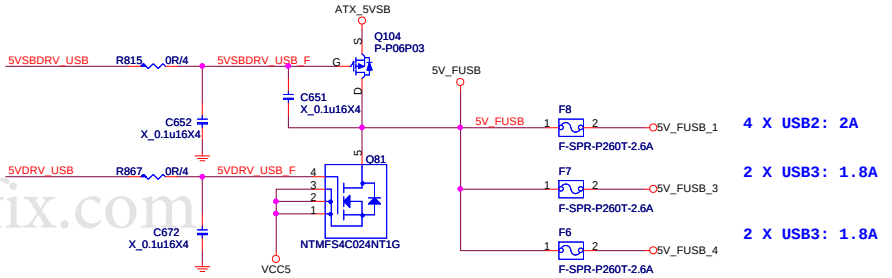
PS2 Keyboard & Mouse Connector



Rear USB Port Power



Front USB Port Power



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MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB Power & PS2	1.0

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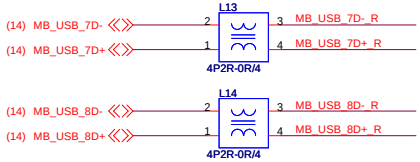
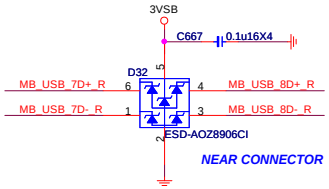
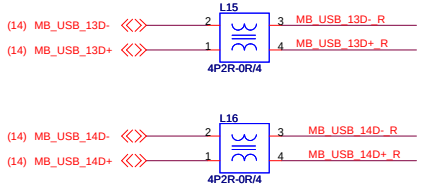
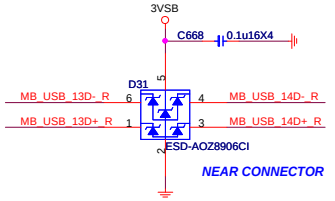
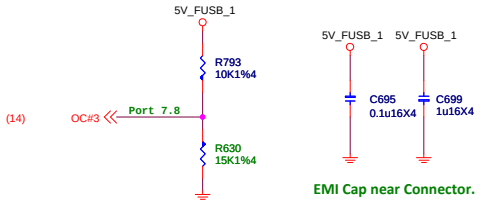
Front USB2.0

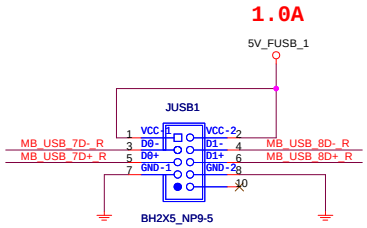


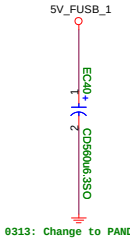


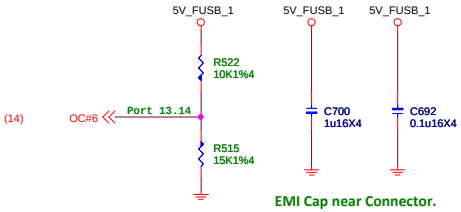


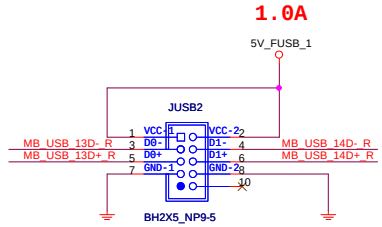












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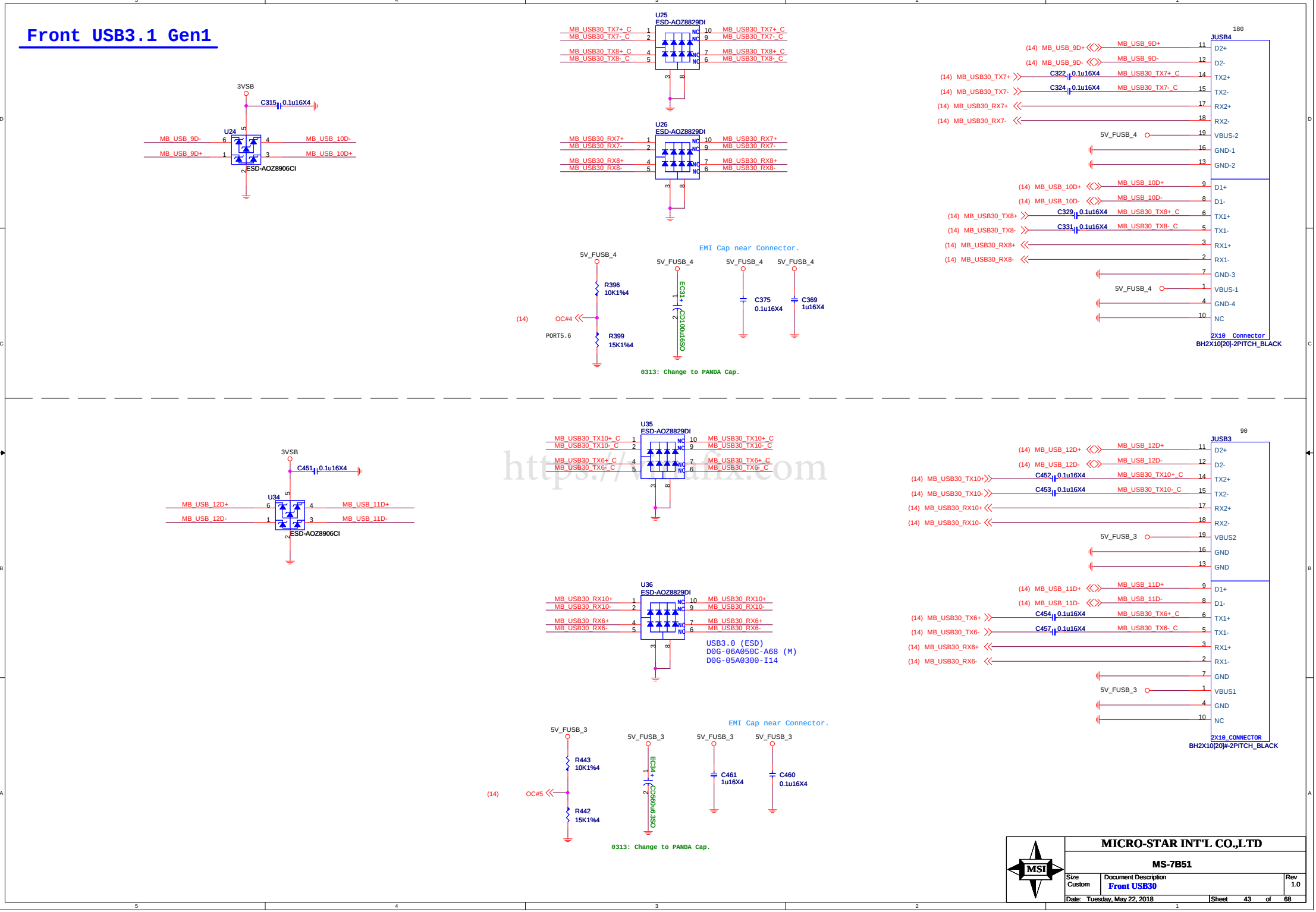
Front USB3.1 Gen1



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MS-7B51

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Custom	Front USB30	1.0

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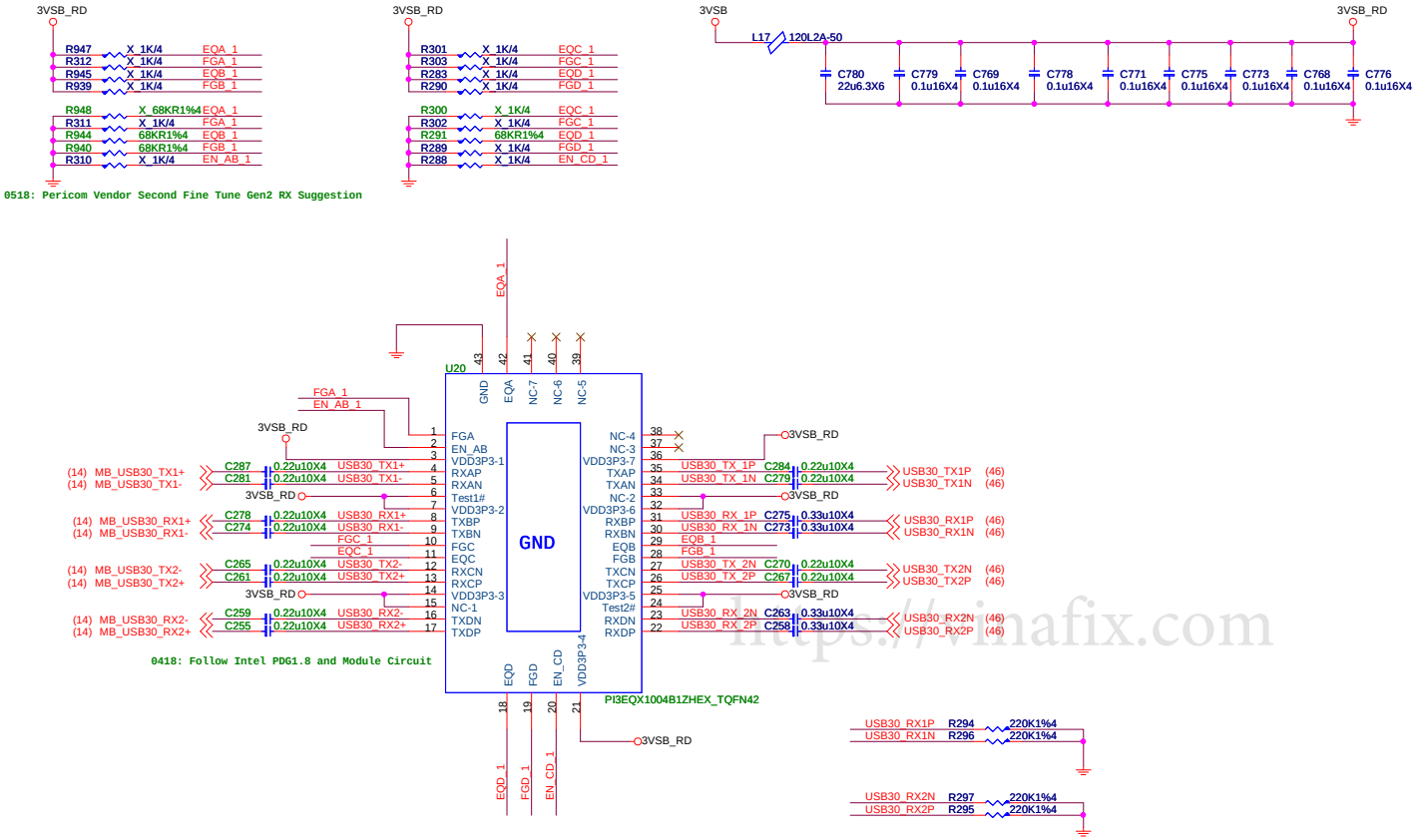
Rear USB3.1 Redriver



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MICRO-STAR INT'L CO.,LTD		
MS-7B51		
Size: Custom	Document Description: Rear USB3.1 Redriver	Rev: 1.0
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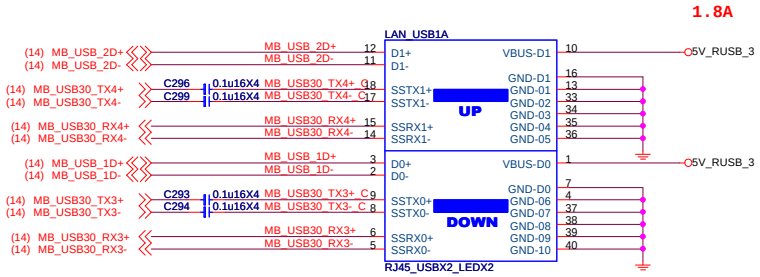
Rear LAN USB3.1 Gen1



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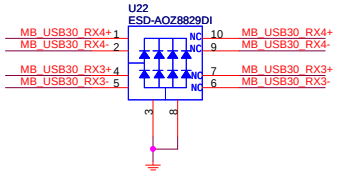

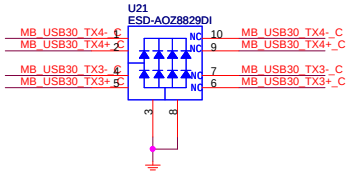

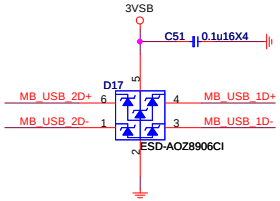

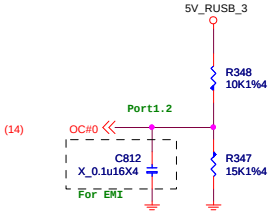

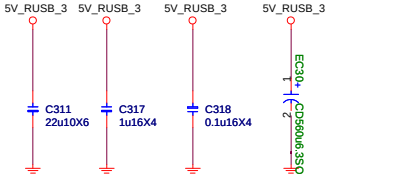

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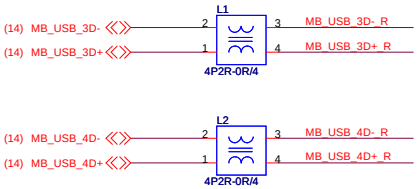
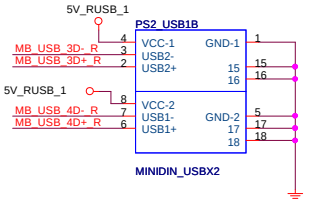
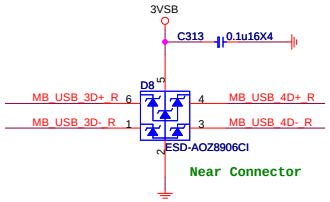
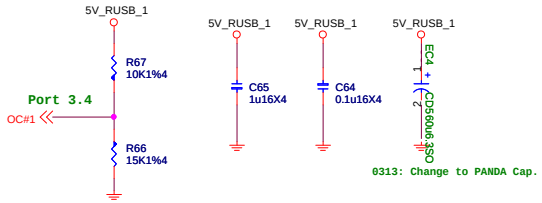
PS2 USB2.0









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MS-7B51		
Size: Custom	Document Description: Real LAN USB3.1/PS2	Rev: 1.0
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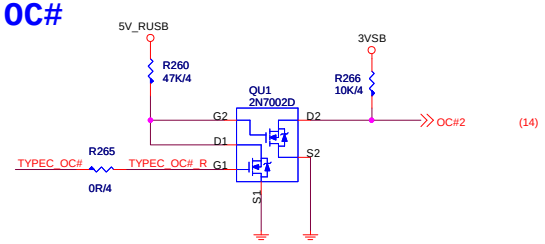
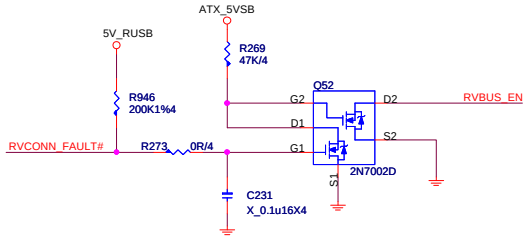
VBUS OC#



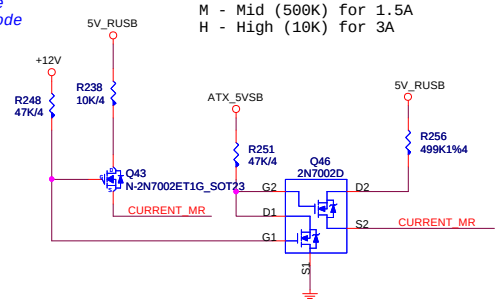
VCONN OC#

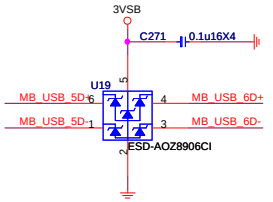


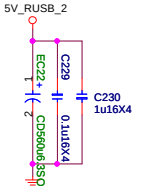
Current Mode

3A under S0 mode
1.5A under S3 mode

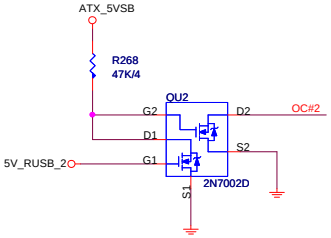
L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

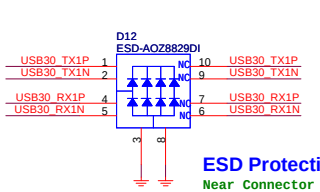




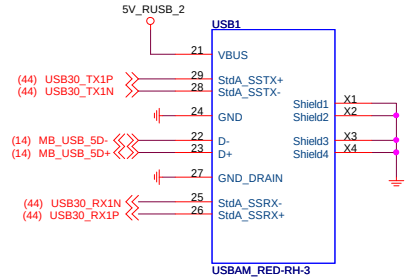


0313: Change to PANDA Cap.





ESD Protection
Near Connector



USB Type-C MUX with Configuration Channel (CC)

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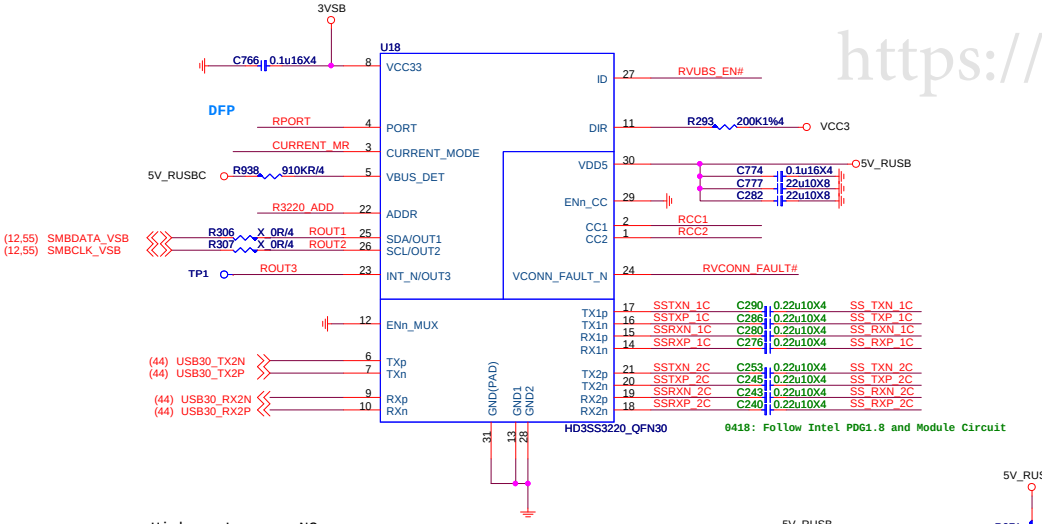
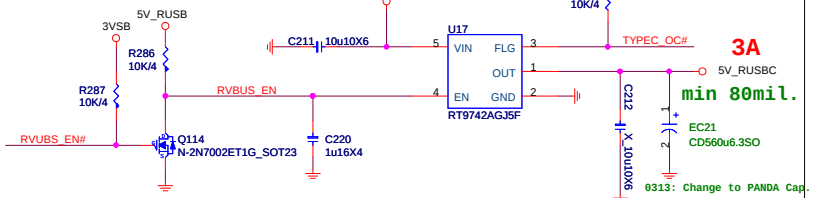


0418: Follow Intel PDG1.8 and Module Circuit

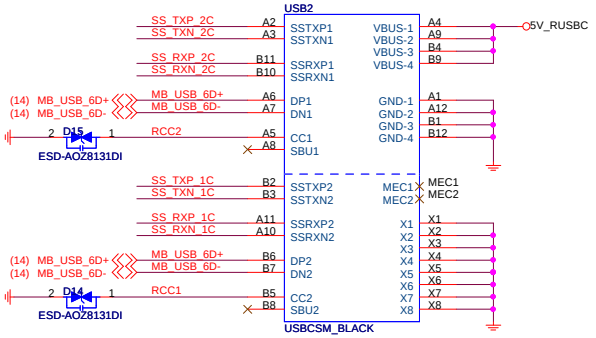
R3220_ ADD	High	Low	NC
RPORT	0x67 DFP(V)	0x47 UFP	GPIO mode(V) DRP



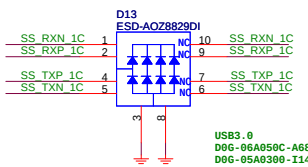
3A
min 80mil.

0313: Change to PANDA Cap.

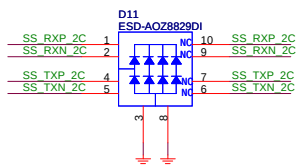
TYPE-C

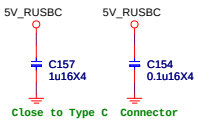


ESD Protection



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL





Close to Type C Connector

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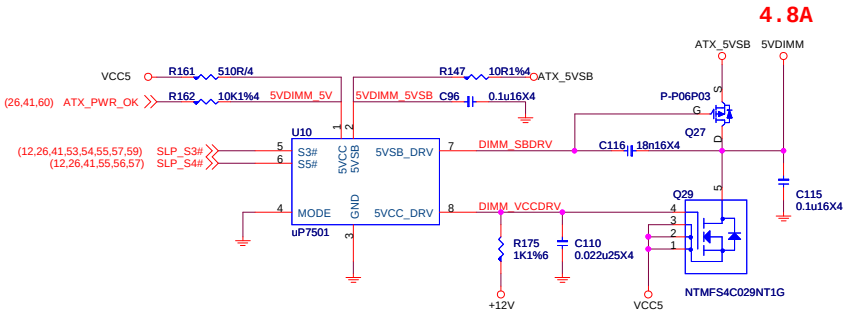
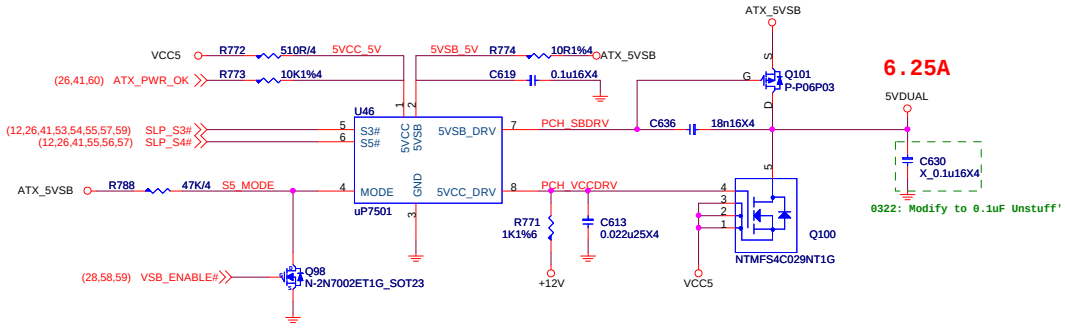
5VDIMM FOR DDR

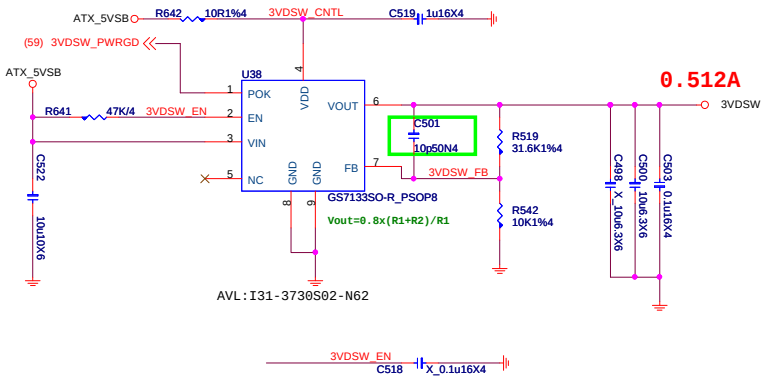


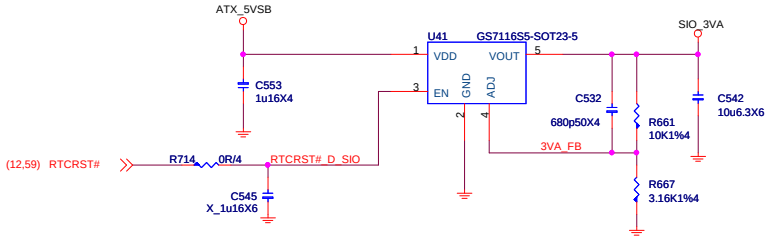
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

5VDUAL

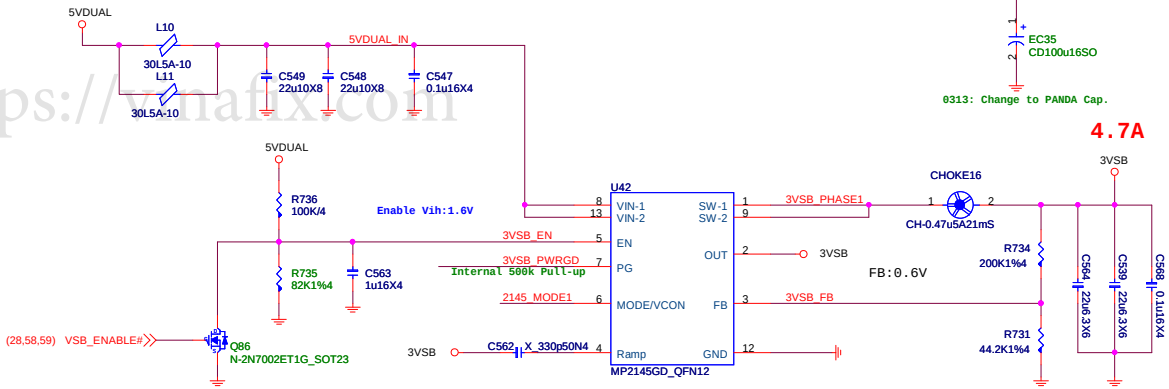


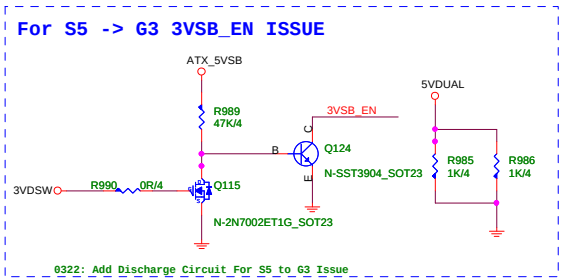
3VDSW

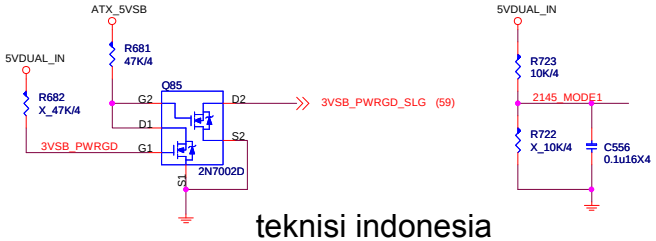




3VSB cost down







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MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B51	
Size: Custom	Document Description: ACPI-MPS	Rev: 1.0
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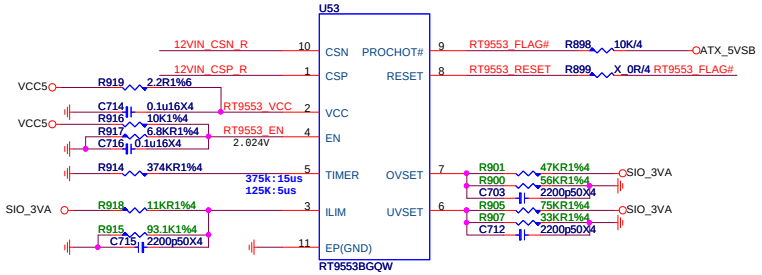
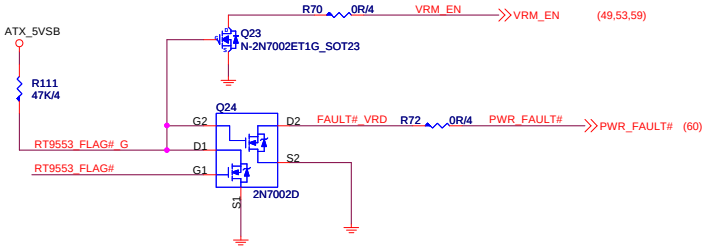
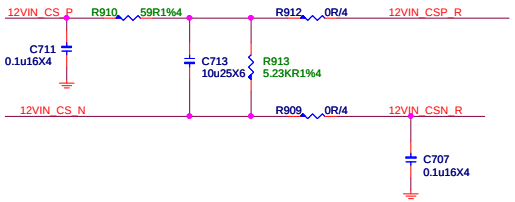
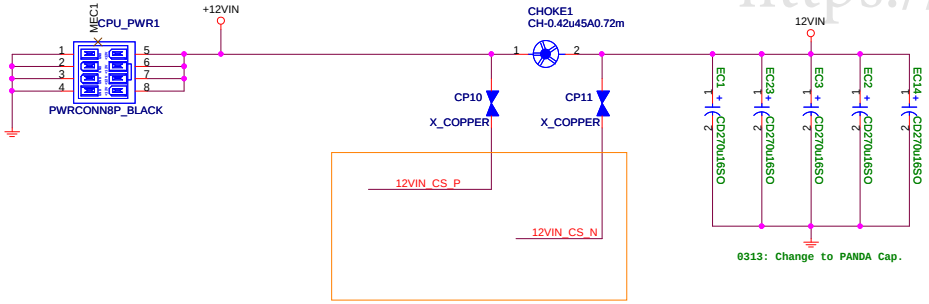
OCP: 45A For 8 core 193A Support

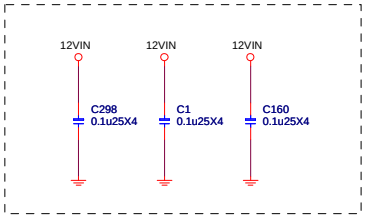




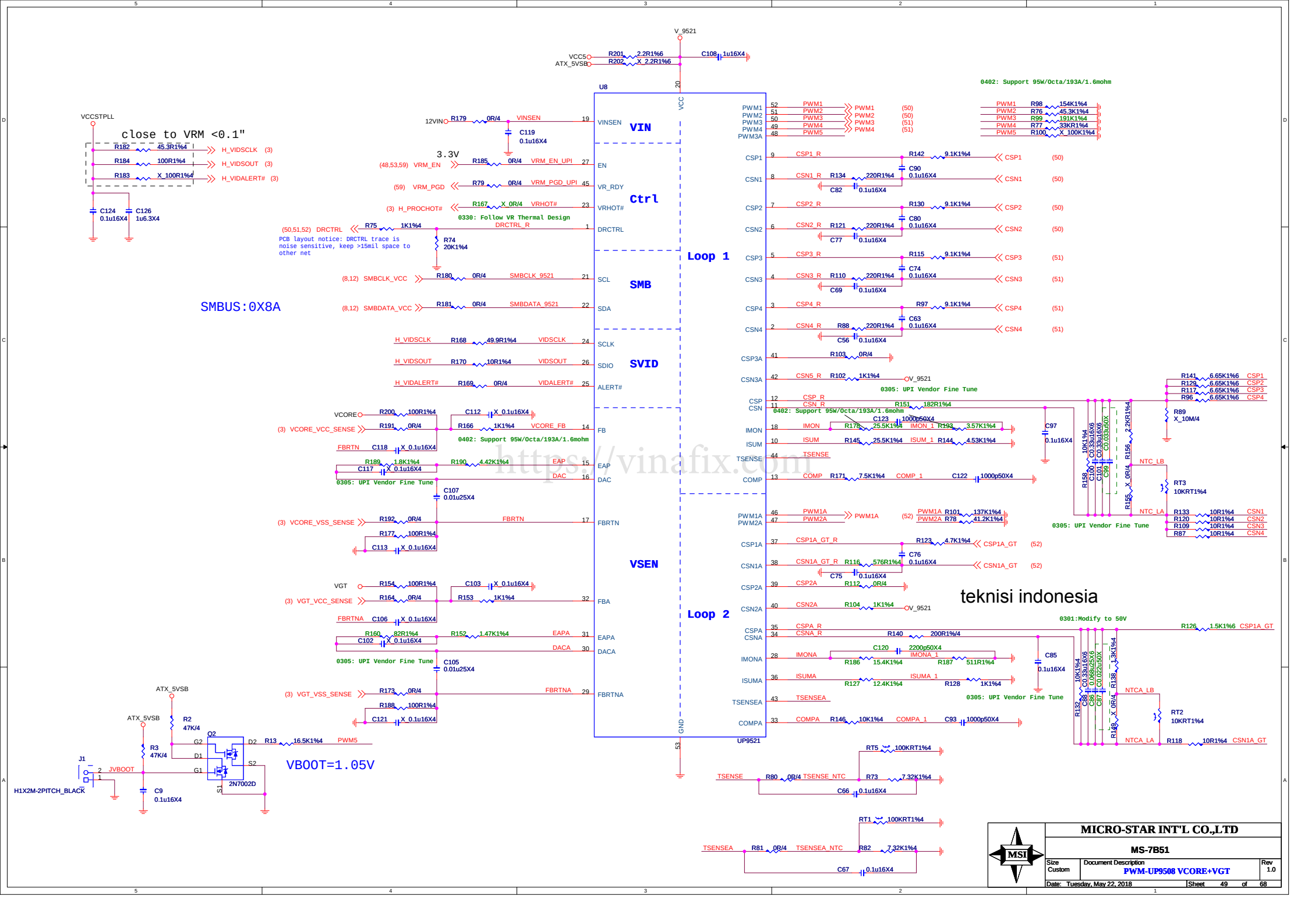


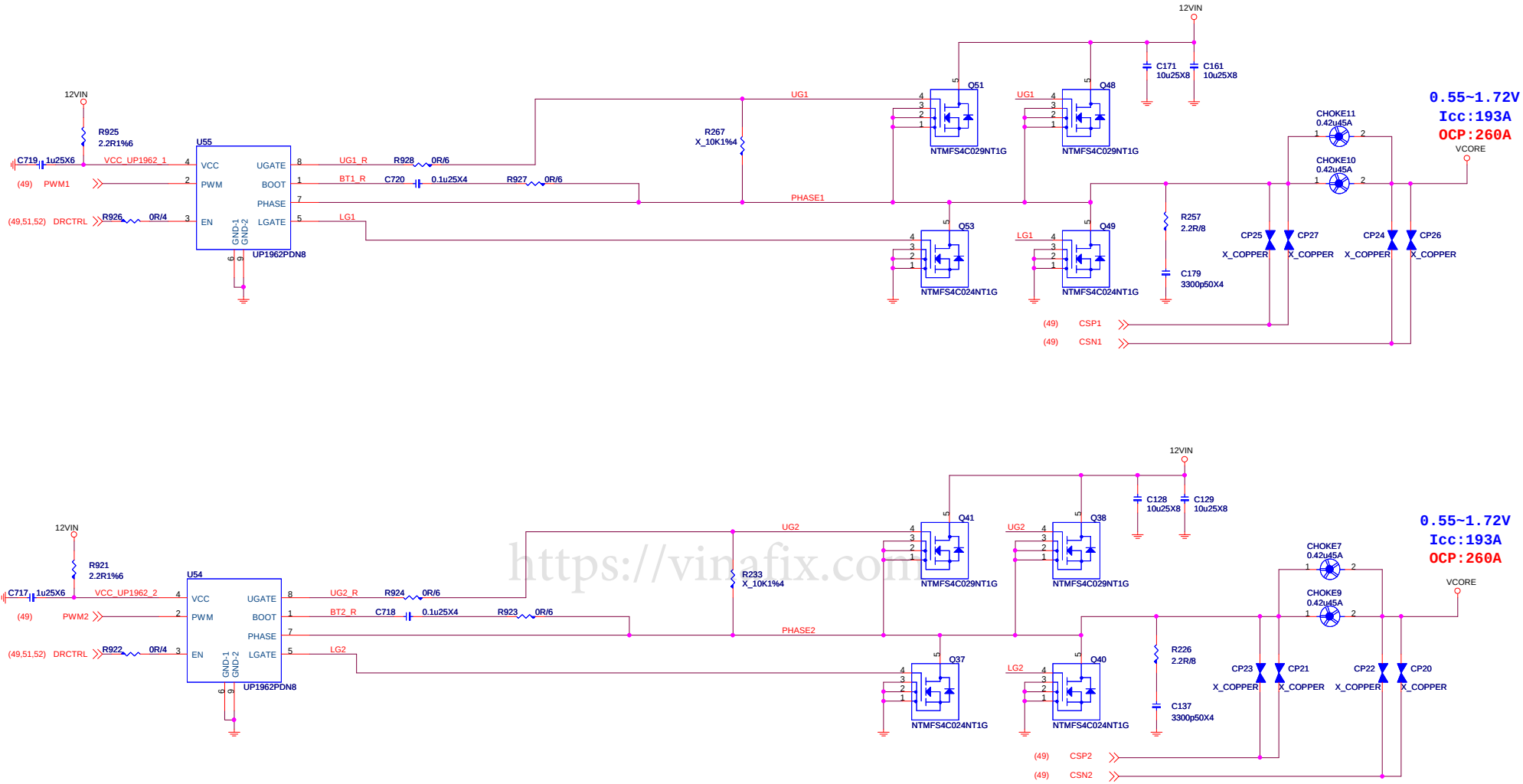
https://vinafix.com





MICRO-STAR INT'L CO.,LTD		
MS-7B51		
Size: Custom	Document Description: Rear I/O PS2	Rev: 1.0
Date: Tuesday, May 22, 2018	Sheet 48 of 68	


close to VRM <0.1"
SMBUS:0X8A
VBOOT=1.05V
U8
UP9521
VIN
Ctrl
SMB
SVID
VSEN
Loop 1
Loop 2
0402: Support 95W/Octa/193A/1.6mohm
0330: Follow VR Thermal Design
0305: UPI Vendor Fine Tune
0301:Modify to 50V
PCB layout notice: DRCTRL trace is noise sensitive, keep >15mil space to other net
teknisi indonesia
MICRO-STAR INT'L CO.,LTD
MS-7B51
PWM-UP9508 VCORE+VGT
Tuesday, May 22, 2018



https://vinafix.com

MICRO-STAR INT'L CO.,LTD		
MS-7B51		
Size: Custom	Document Description: VCORE MOS-PHASE 1~2	Rev: 1.0
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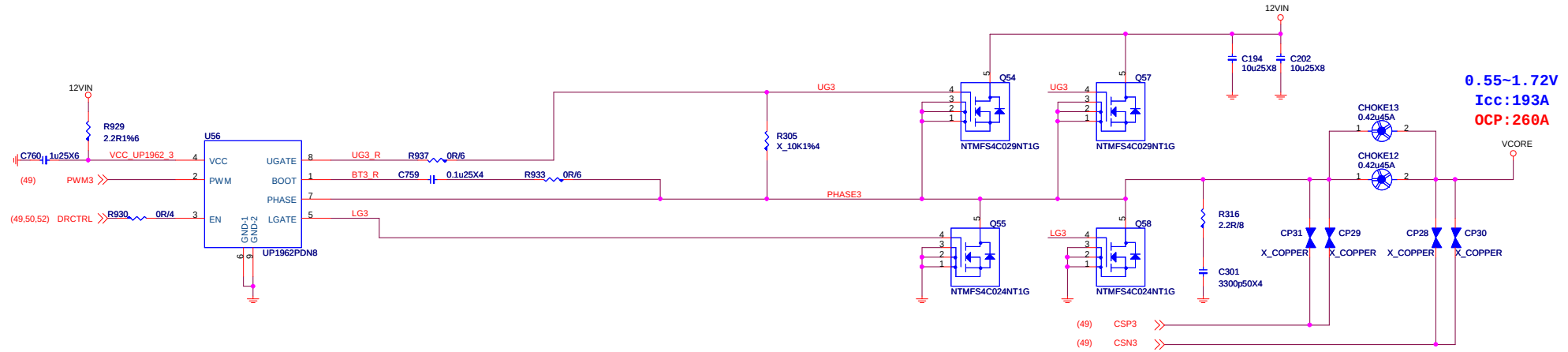
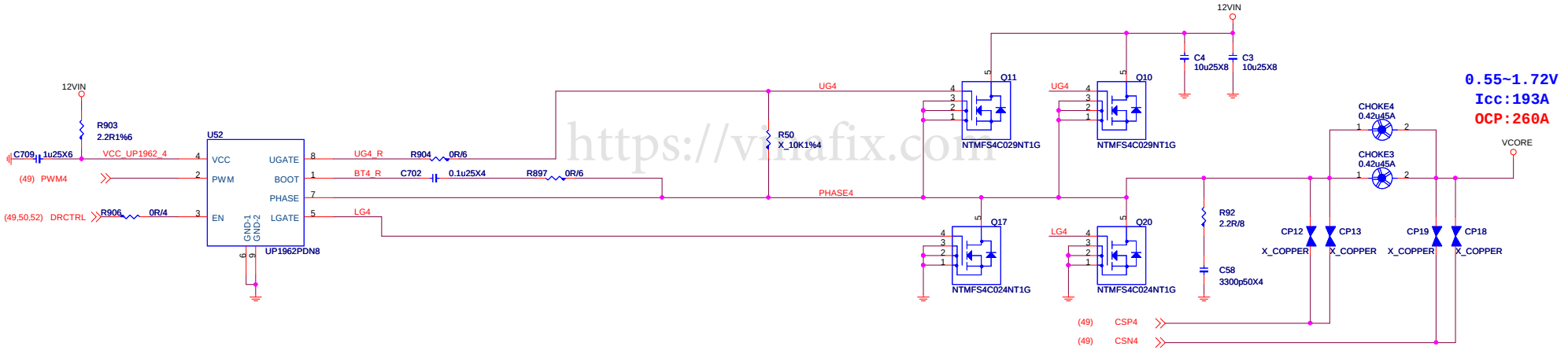
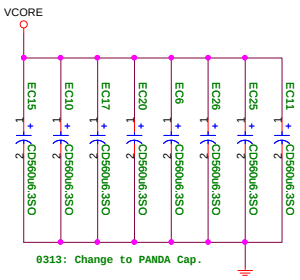


Vinafix.com



https://vinafix.com



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	VCORE MOS-PHASE 3~4	1.0

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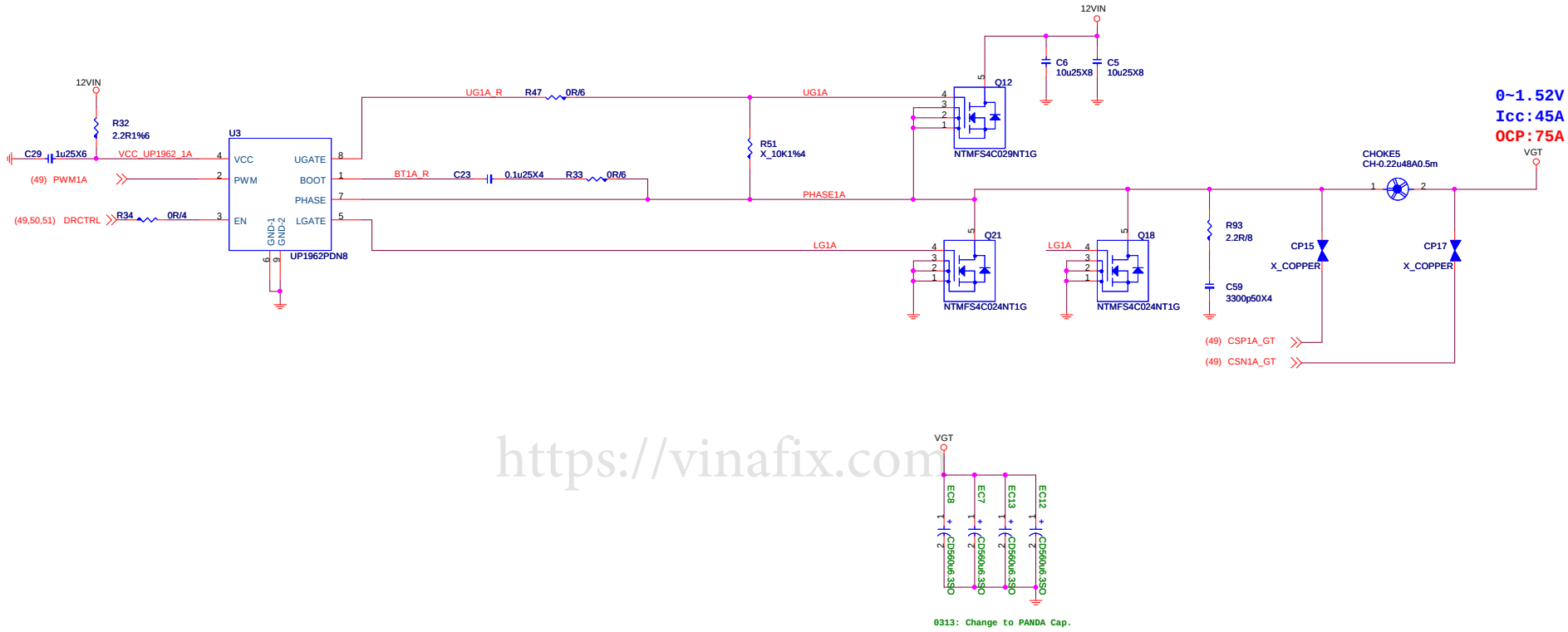

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0313: Change to PANDA Cap.

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: VGT MOS-PHASE 1~2	Rev: 1.0
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SA Power:1.05V,11.1A

OCP = 14.43A; Choke Isat=14A

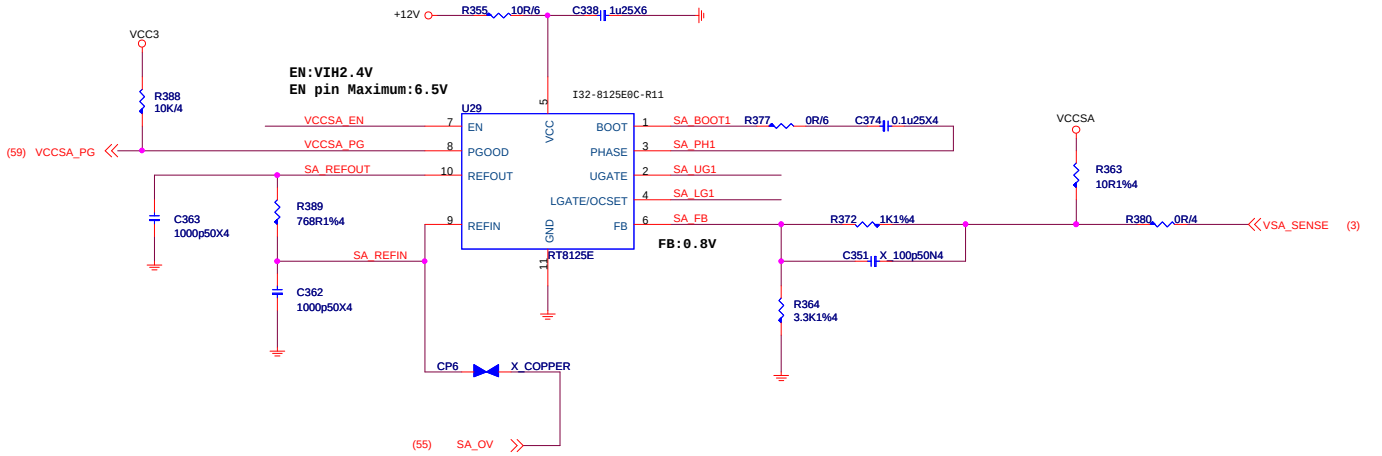
Rocset = 1.3 * Imax * Rdson(low) / Iocset
R343 = 1.3 * 11.1 * 2.3mohm / 10uA
R343 = 3.31K (小於5K, 取接近值5.1K)

Rdson(Low Side) 10V
D03-4C02403-005:2.3 ~2.8 mohm

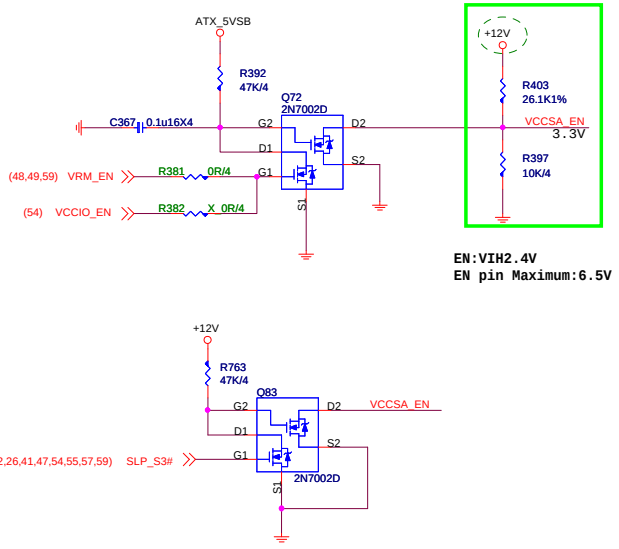
$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

OCP MOSFET

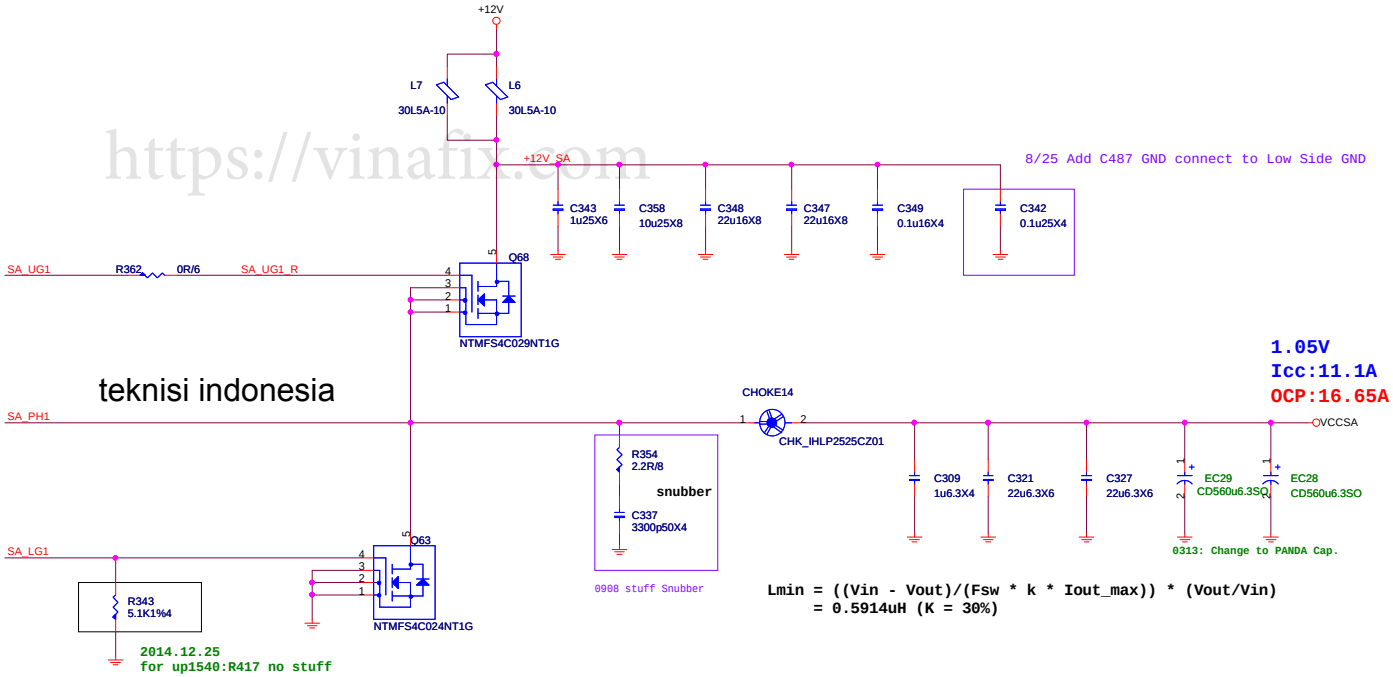
Current Sensing				
IOCSET	9	10	11	μA



Pull up by layout&Check level



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
SLP_S3# assertion to VR disabled
max:1us



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

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MICRO-STAR INT'L CO.,LTD		
MS-7B51		
Size: Custom	Document Description: CPU PWR-VCCSA-PV3205Q	Rev: 1.0
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VccIO Power

IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

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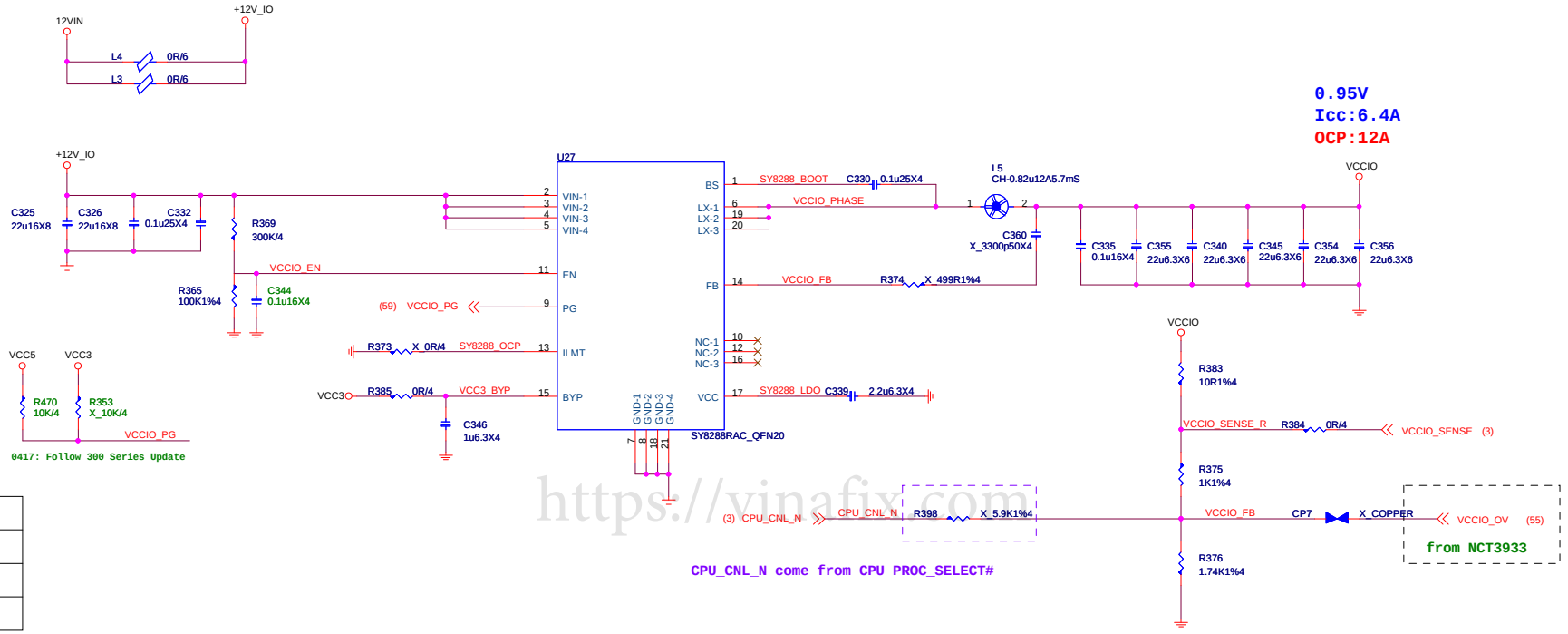
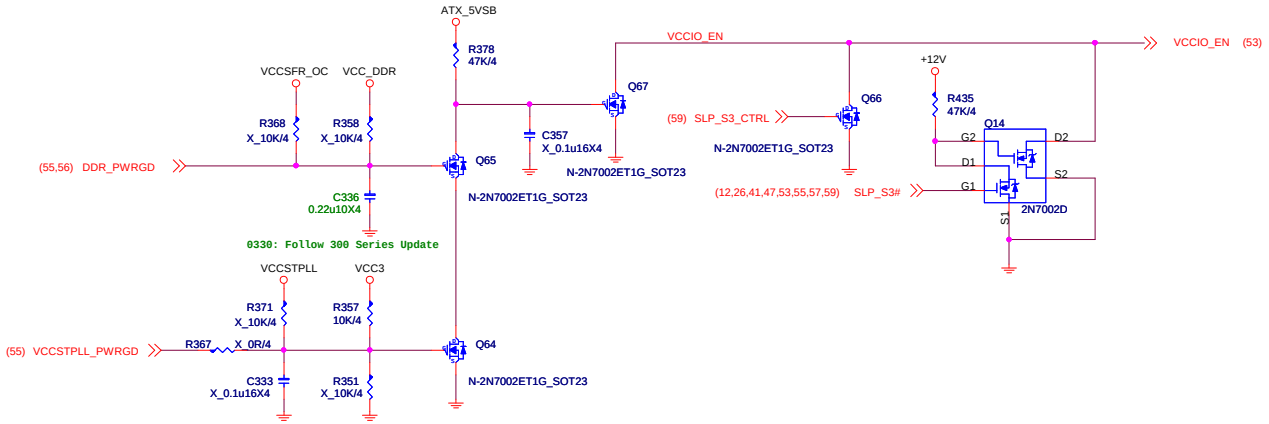


SY8288_OCP	OCP
0	8A
Floating	12A
1	16A



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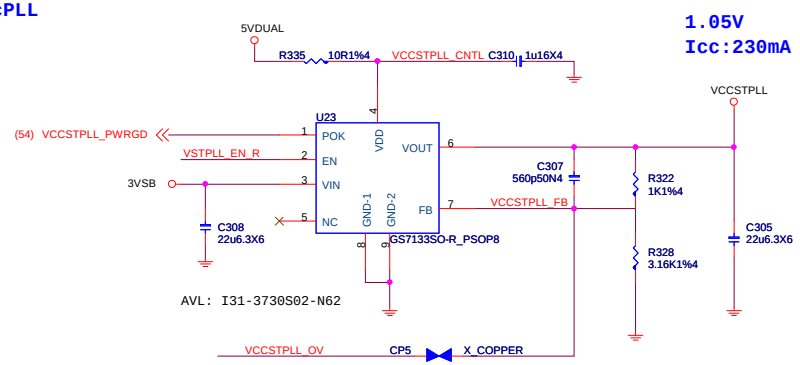
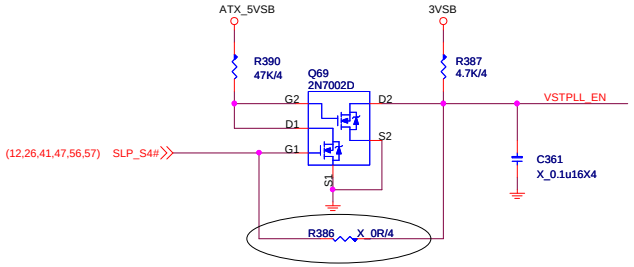
MICRO-STAR INT'L CO.,LTD	
MS-7B51	
Size: Custom	Document Description: CPU PWR-VCCIO-NB685
Rev: 1.0	
Date: Tuesday, May 22, 2018	Sheet 54 of 68

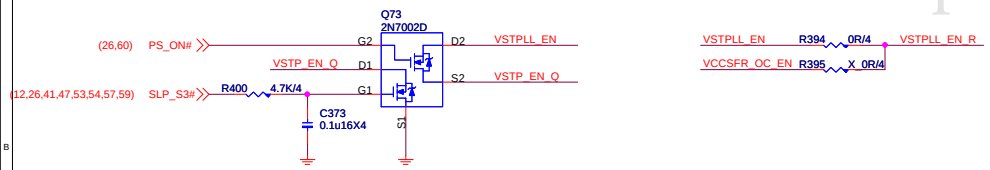
VccST+VccPLL

80mA For VccST
150mA For VccPLL

1.05V
Icc:230mA



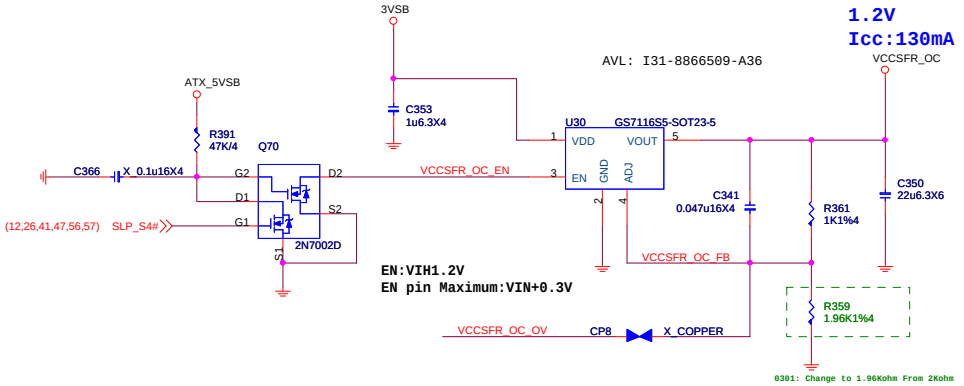




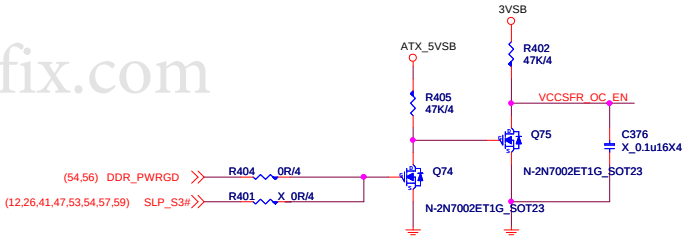
VCCPLL_OC

1.2V
Icc:130mA

AVL: I31-8866509-A36



EN:VIH1.2V
EN pin Maximum:VIN+0.3V



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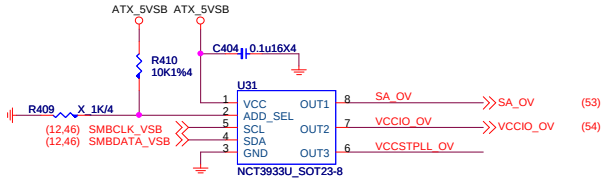
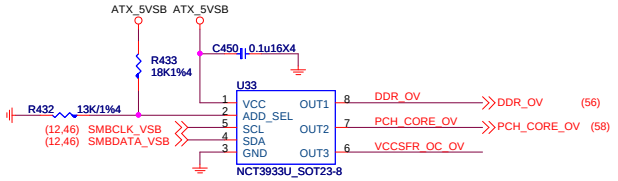
VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



0x26:RH=18K,RL=13K



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Custom	CPU PWR-VCCST/PLL	1.0

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DDR4 Power:1.2V,19.7A *OCP:28A*

3.3A For CPU
15.7A For 4DIMM
0.7A For DDR VTT

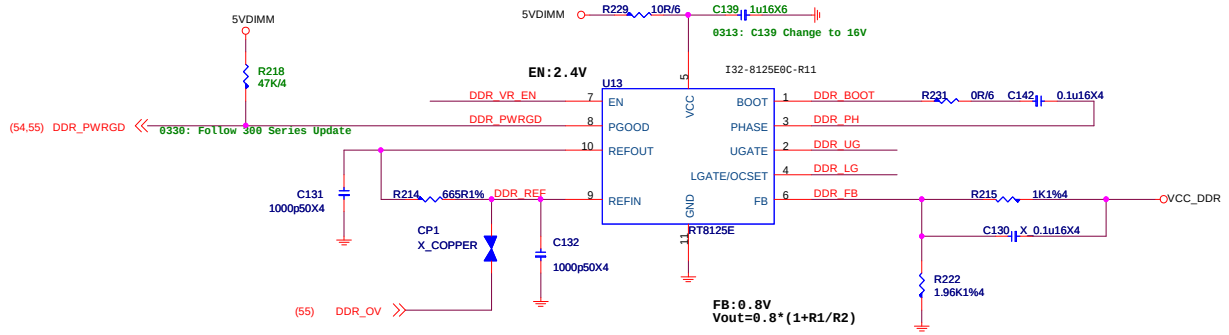
OCP = 29.55A; Choke Isat=30A

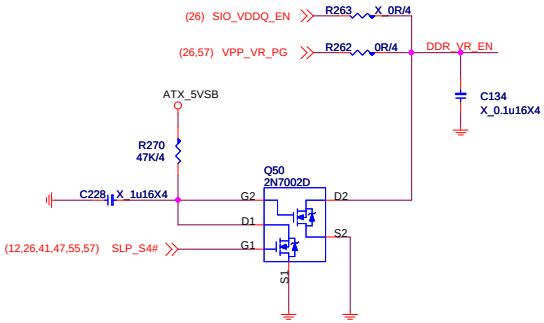
```
Rocset = 1.5 * Imax * Rdson(low) / Iocset
R230   = 1.5 * 19.7 * 3.3mohm / 10uA
R230   = 9.75K
```

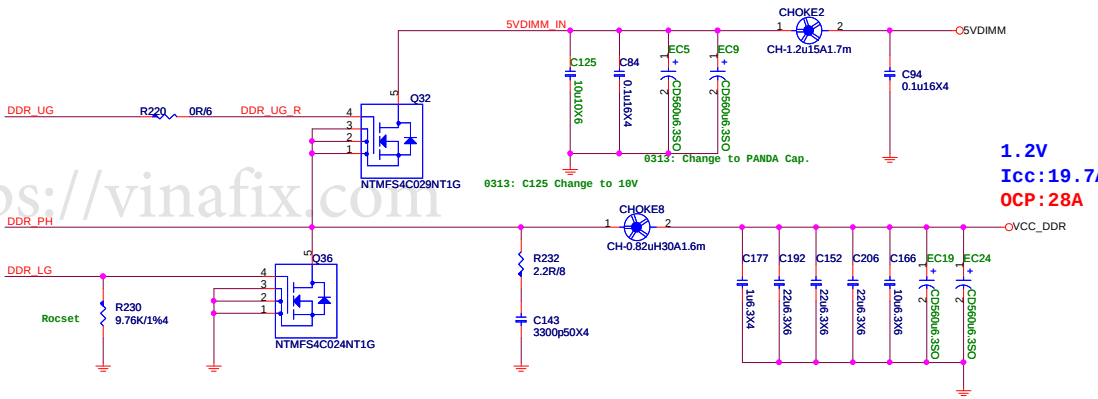
Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~ 4mohm

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$ (OCP: MOSFET)

Current Sensing					
Iocset			9	10	11	uA







1.2V
Icc:19.7A
OCP:28A

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MS-7B51	
Size: Custom	Document Description: DDR4 Power-RT8125
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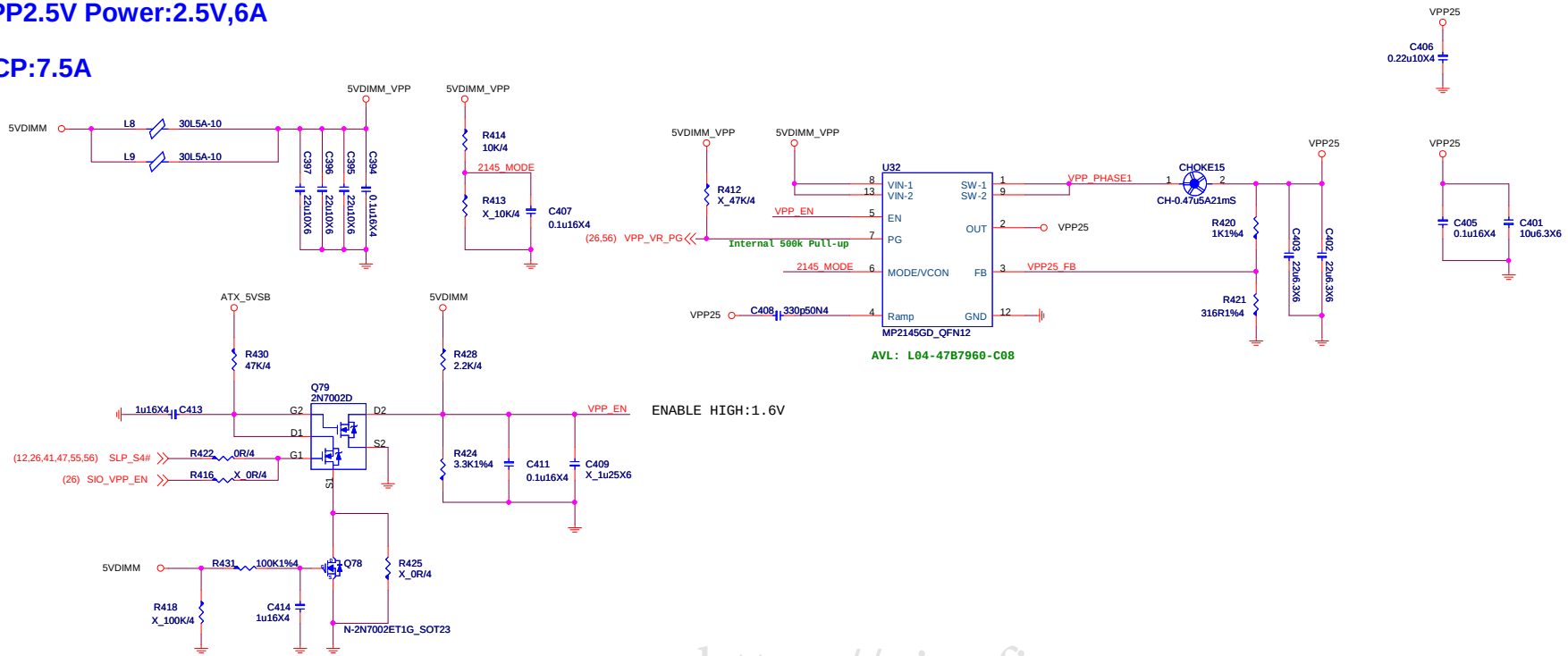
VPP2.5V Power:2.5V,6A

OCP:7.5A



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DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

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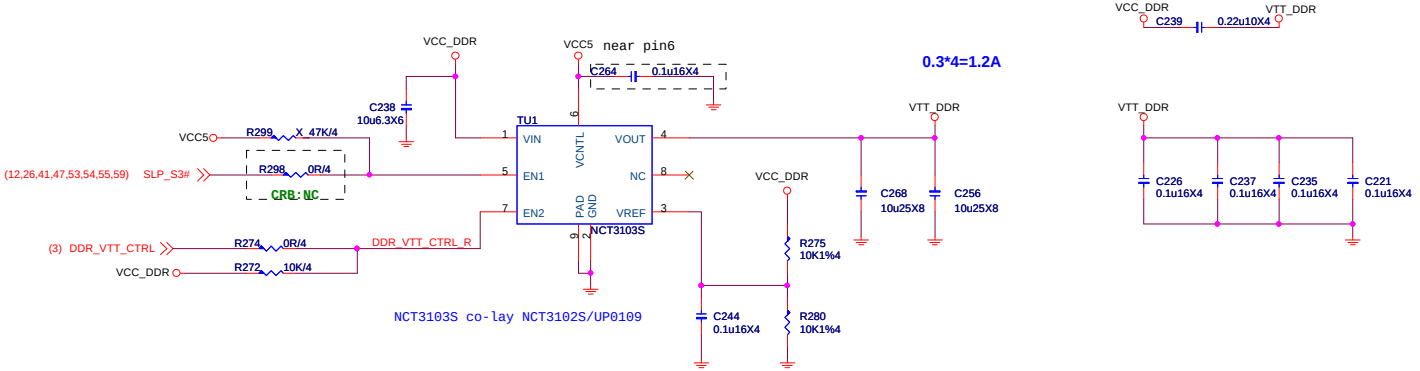

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B51	
Size: Custom	Document Description: DDR PWR VPP25/VTT-MP2145	Rev: 1.0
Date: Tuesday, May 22, 2018	Sheet 57 of 68	

PCH_1VSB Power:1.05V,14A

OCP = 17.862A

```
Rocset = 1.3 * Imax * Rdson(low) / Iocset
R784   = 1.3 * 13.74 * 3.3mohm / 10uA
R784   = 5.89K
```

Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~4 mohm

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

OCP — MOSFET

Current Sensing

IOCSET			9	10	11	14

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 10.664 * 0.4
     = 4.2656A < 5000mA
```

5VDUAL
R785 10R/6
C626 1u16X6
PCH_1VSB_EN
U45 RT8125E
0313: C626 Change to 16V
EN PGOOD REFOUT REFIN VCC GND BOOT PHASE UGATE LGATE/OCSET FB
PCH_BOOT R777 0R/6 PCH_R_BOOT C620 0.1u25X4
PCH_PHASE
PCH_UGATE R789 0R/6 PCH_R_UGATE
PCH_LGATE
(59) 1P05VSB_PG
PCH_REFOUT
PCH_REFIN
C610 1000p50X4
R770 768R1%4
C611 1000p50X4
CP9 X_COPPER
(55) PCH_CORE_OV
Rocset R784 5.9K1%4
PCH_CORE_FB_R
C624 X_0.01u25X4 PCH_TYPE3 R781 X_0R/4
R780 1K1%4 PCH_CORE_FB
R779 3.09K1%4
0301: Change to 3.09Kohm From 3.16Kohm

```
Vout = Vref * (1 + R821/R822)
     = 0.8 * (1 + 1K/3.92K)
     = 0.8 * 1.2551
     = 1.004V
```

5VDUAL_PCH_IN
C614 0.1u16X4
C612 10u25X8
EC38 CD560u6.3SO
C631 X_0.1u25X4
CHOKE18 CH-0.47u5A21mS
5VDUAL
C629 X_0.1u16X4
0322: Modify to 0.1uF Unstuff'
Q93 NTMFS4C029NT1G
Q94 NTMFS4C024NT1G
R783 2.2R/8
C628 3300p50X4
CHOKE17 CH-0.82u18A4.6mS
PCH_1P05_VSB
EC37 CD560u6.3SO
EC36 CD560u6.3SO
C584 22u6.3X6
C596 10u6.3X6
C595 10u6.3X6
C598 1u6.3X4
0313: Change to PANDA Cap.
R776 0R/4
R775 X_0R/4
PCH_MPHY_SENSE (16)

```
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
     = 0.8335uH (K = 30%)
```

5VDUAL
R786 47K/4
PCH_1VSB_EN
C615 X_0.1u16X4
ATX_5VSB
R787 47K/4
Q96 N-2N7002ET1G_SOT23
C627 X_0.1u16X4
PCH_1P8_VSB
R791 1K1%4
Q97 N-SST3904_SOT23
3VSB
R792 X_10K/4
R790 X_2.21K1%4
PCH_1VSB_EN
(28,47,59) VSB_ENABLE#
Q99 N-2N7002ET1G_SOT23

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1P8V_VSB

ATX_5VSB
3VSB
R1021 X_10R1%4 1P8_VSB_CNTL C618 X_1u16X4
R1020 X_47K/4
U44 X_GS7133SO-R_PSOP8
POK EN VIN NC VDD VOUT FB GND-1 GND-2
(59) 1P8_VSB_PG
1P8_VSB_EN
3VSB
C605 X_220p50N
R1022 X_15K1%4
1P8_VSB_FB
R1023 X_11.3K1%4
0301: Change to 11.3Kohm From 12Kohm
C608 X_10u6.3X6
C607 X_10u6.3X6
C632 X_0.1u16X4
1P8_VSB
(28,47,59) VSB_ENABLE#
Q122 X_N-2N7002ET1G_SOT23
C616 X_0.1u16X4
C617 X_10u6.3X6
FB=0.8V

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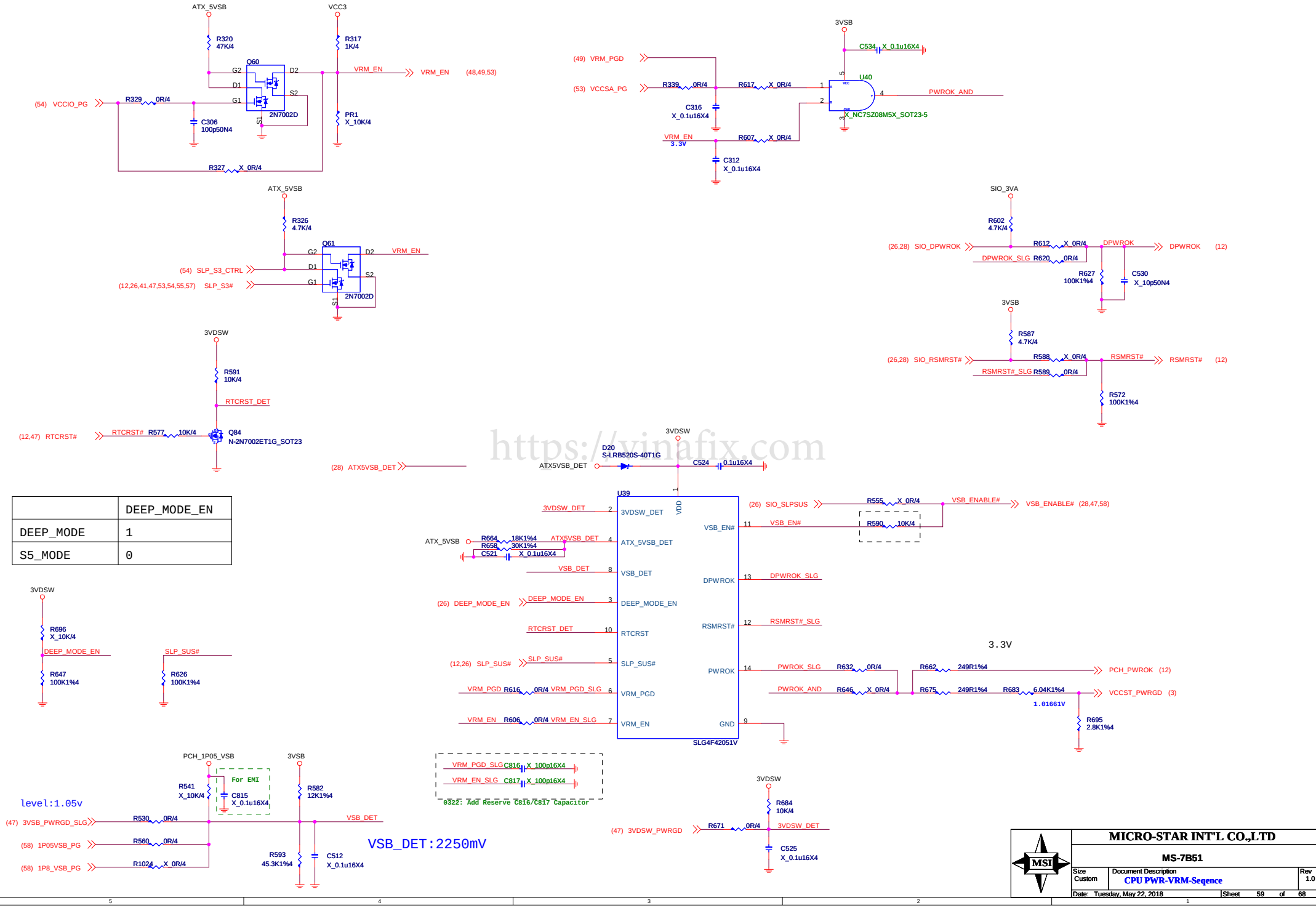

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

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MICRO-STAR INT'L CO.,LTD

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Custom	CPU PWR-VRM-Seqence	1.0

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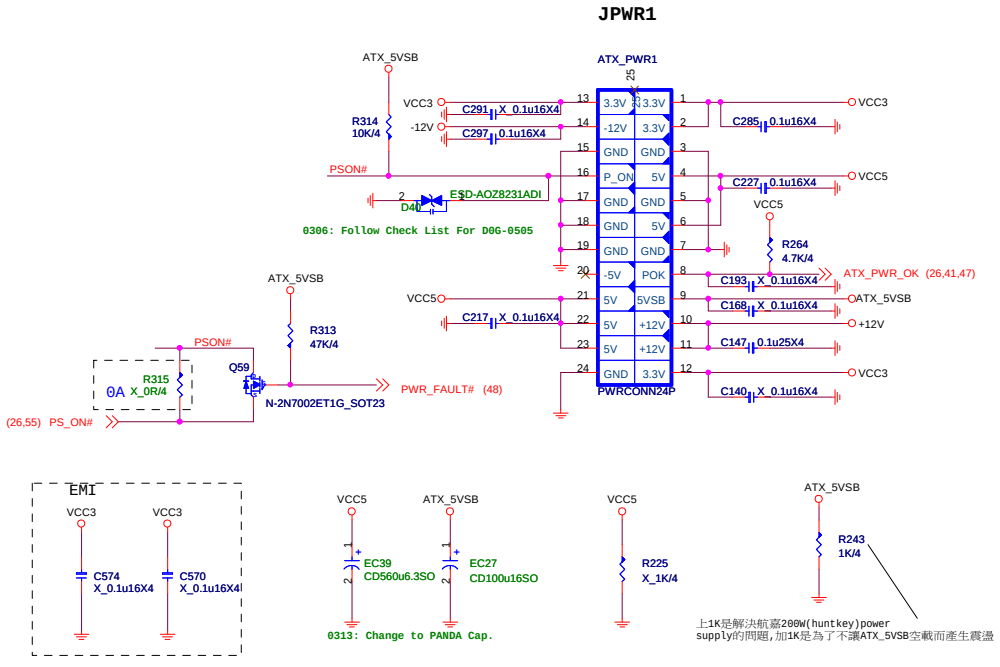
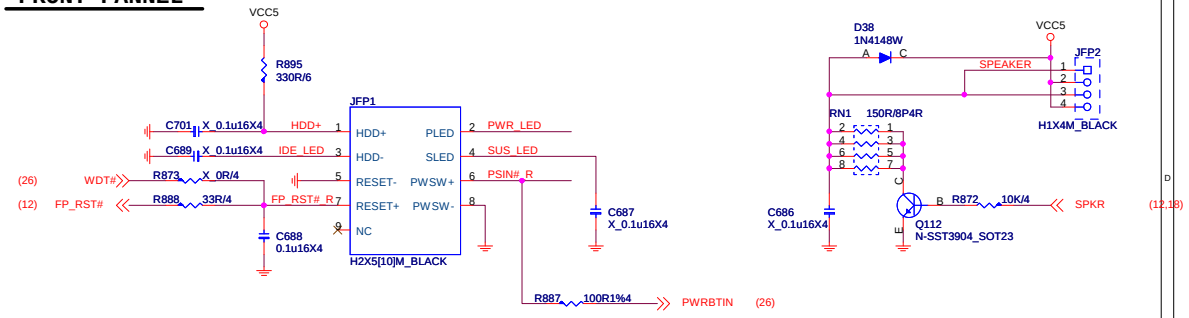
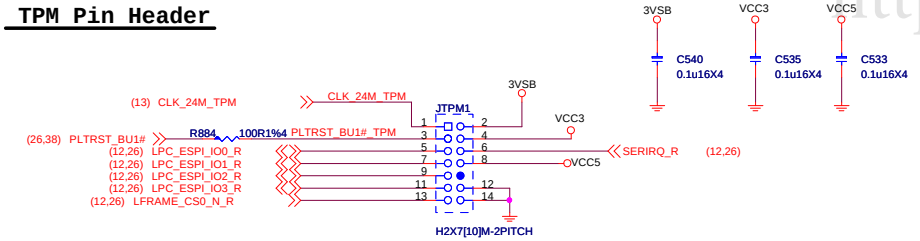
ATX POWER CONNECTOR



FRONT PANNEL

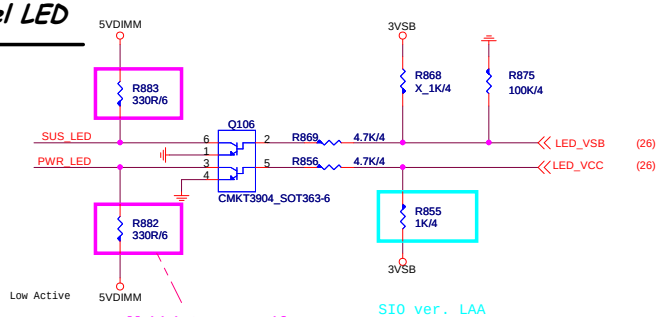


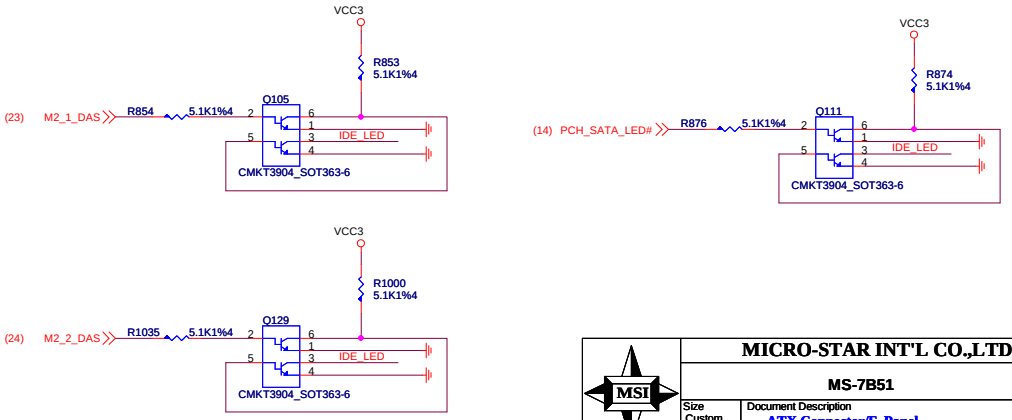
TPM Pin Header



https://vinafix.com

Front Panel LED





MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ATX Connector/F_Panel	1.0

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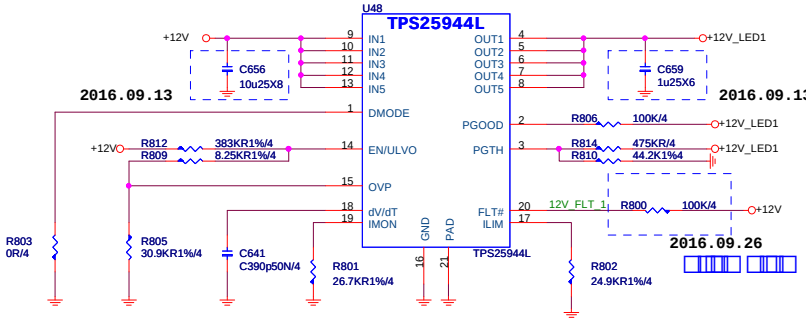
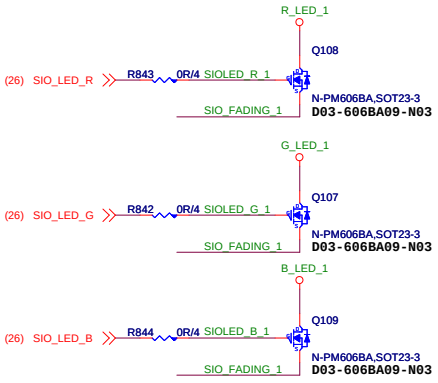
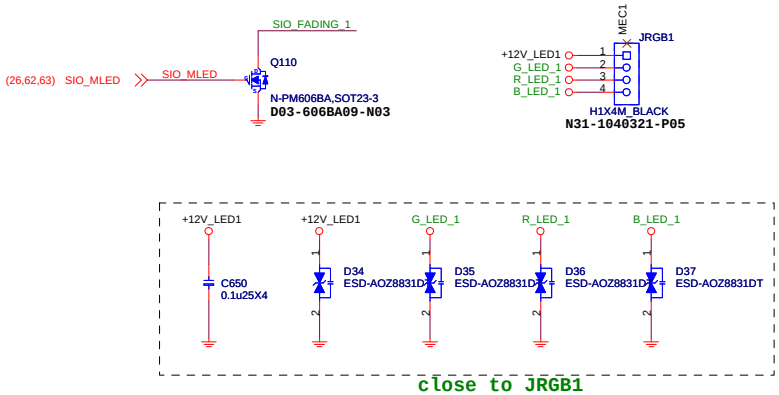
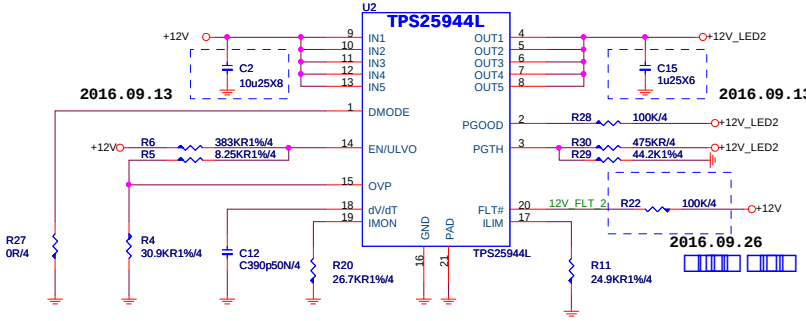
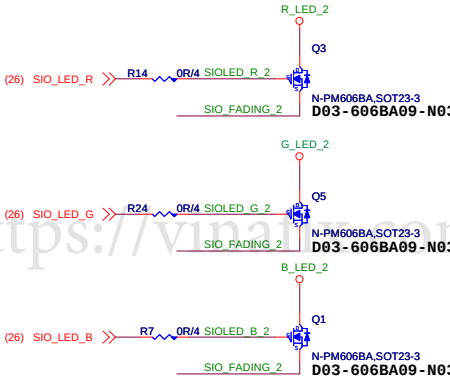
StripLine LED

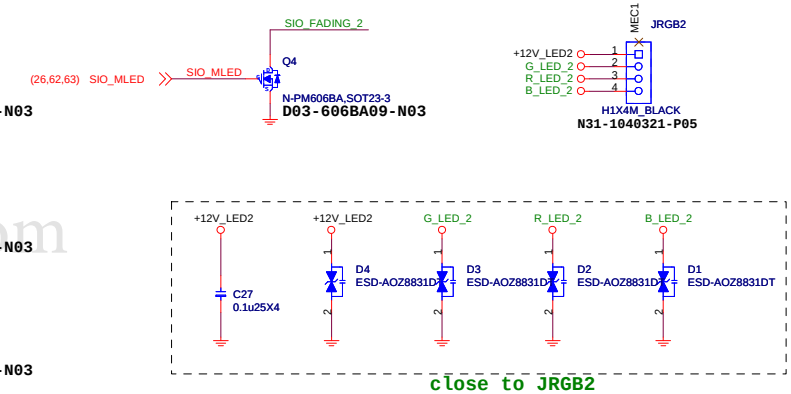












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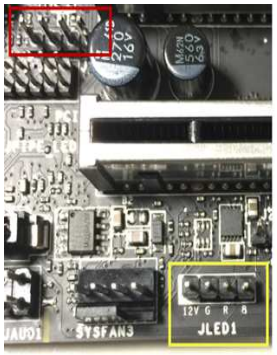
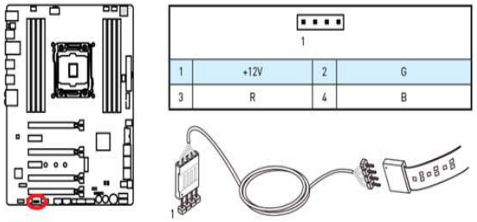


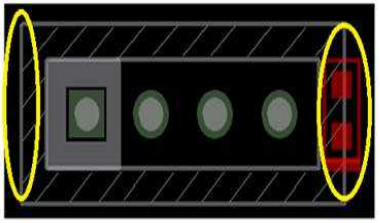
JLED1: RGB LED connector

This connector allows you to connect the RGB LED strip.

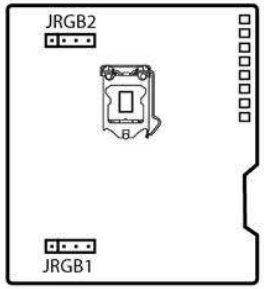


Important

- This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.
- Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.
- Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.



JLED1電源督示燈請擺在旁側



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MS-7B51		
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Sidebar LED x 12

MKT Name LED x 10

VCC5 — SIDE_LED1 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED2 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED3 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED4 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED5 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED6 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED7 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED8 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED9 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED10 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED11 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED12 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED13 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED14 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED15 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED16 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED17 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED18 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED19 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED20 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED21 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V
VCC5 — SIDE_LED22 — SIDEBAR_R_LED — LED04-[BR]-25mA2.35V

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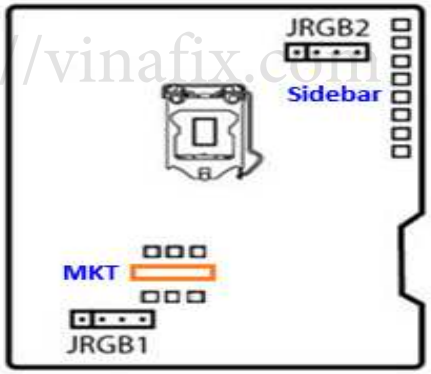
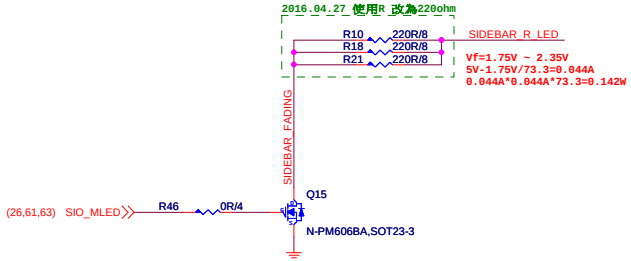


LED SIDEBAR CONTROL

G:11.5mA
B:7.7mA



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Custom	Sidebar LED	1.0

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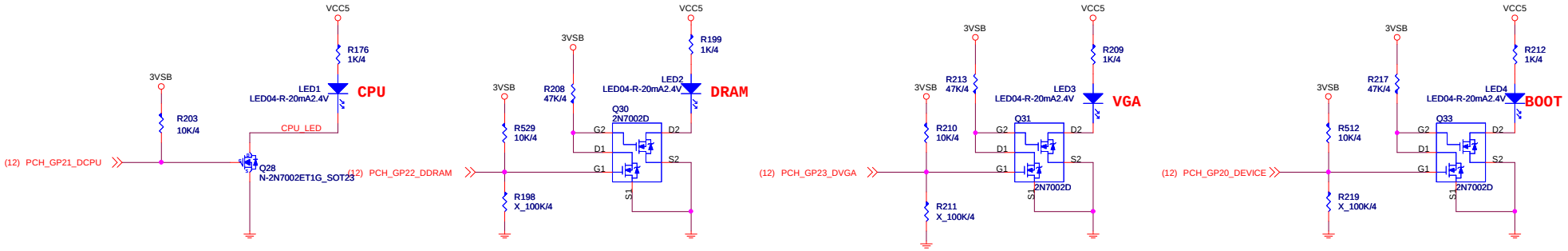
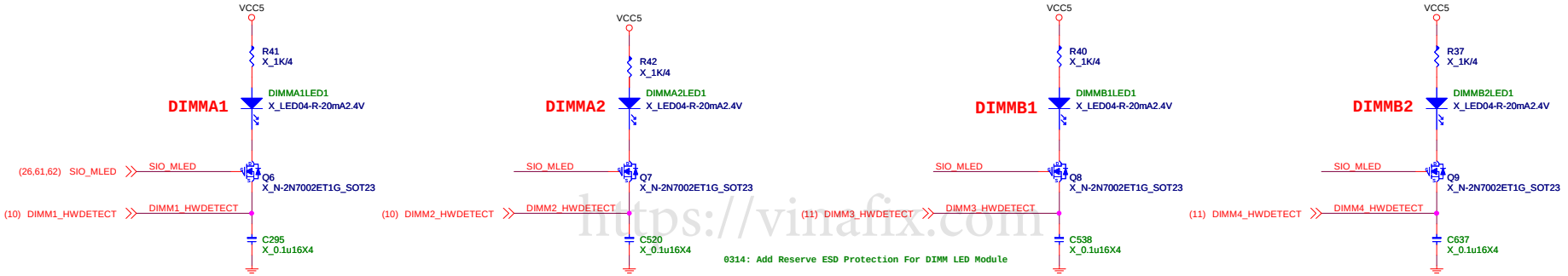
EZ Debug LED



DIMM SLOT LED



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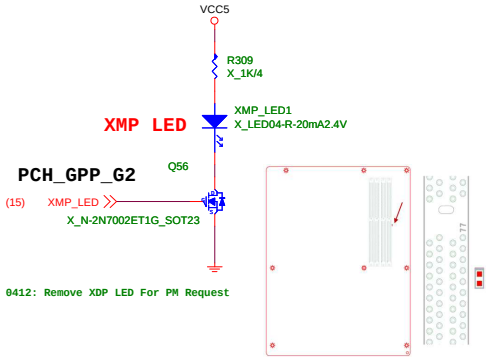
0314: Add Reserve ESD Protection For DIMM LED Module

PCI-E SLOT LED

0410: PM Update Spec

0507: Remove All PCI-E LED

XMP LED



0412: Remove XDP LED For PM Request

MSI	MICRO-STAR INT'L CO.,LTD	
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PCB1

7B51-1.0

CPU_H1

CPU
鐵座

CPU_H1

BAT1_X1

BAT-BCR2032P

Heat Sink

HS_PCH1

MOS_N

OE3-7B51004-K08

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VCC3 C645 X_0.1u16X4
VCC3 C671 X_0.1u16X4
VCC3 C646 X_0.1u16X4
VCC3 C600 X_0.1u16X4
VCC5 C806 X_0.1u16X4
VCC5 C807 X_0.1u16X4
VCC5 C808 X_0.1u16X4
VCC5 C809 X_0.1u16X4
5V_RUSBC C810 X_0.1u16X4

For EMC Request

Mounting Holes

MH1 X_MH001
MH2 X_MH001
MH3 X_MH001
MH6 X_MH001
MH5 X_MH001
MH9 X_MH001
MH7 X_MH001
MH8 X_MH001
MH4 X_MH001

C644 0.1u16X4
C673 0.1u16X4

Simulation

SIM1 X_PIN1*2
SIM2 X_PIN1*2

Optical Fiducial Marks-120

FM7 X_FM
FM2 X_FM
FM3 X_FM
FM1 X_FM
FM5 X_FM
FM4 X_FM
FM8 X_FM
FM6 X_FM

VCORE — VCORE1
VGT — GT1
VCCSA — VCCSA1
VCCIO — VCCIO1
VCC_DDR — VCC_DDR1
VTT_DDR — VTT_DDR1
PCH_1P05_VSB — PCH_1VSB1
5VDUAL — 5VDUAL1
5VDIMM — 5VDIMM1
3VSB — 3VSB1
VBAT — VBAT1
VPP25 — VPP1

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Rev: 1.0
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